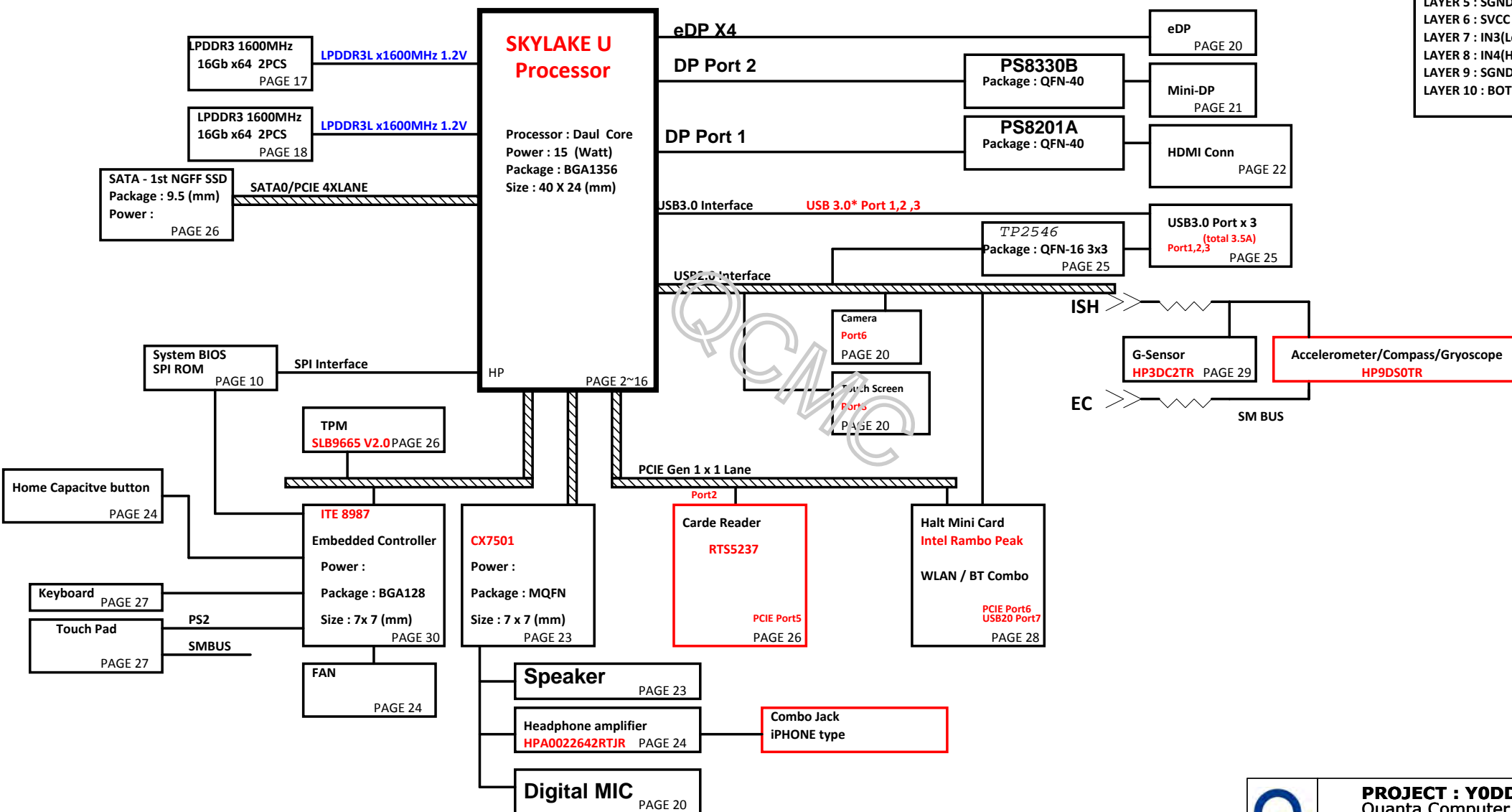


# Pike Intel SKYLAKE ULT Platform Block Diagram

PCB 10L STACK UP

LAYER 1 : TOP  
 LAYER 2 : SGND  
 LAYER 3 : IN1(High)  
 LAYER 4 : IN2(High)  
 LAYER 5 : SGND  
 LAYER 6 : SVCC  
 LAYER 7 : IN3(Low)  
 LAYER 8 : IN4(High)  
 LAYER 9 : SGND  
 LAYER 10 : BOT

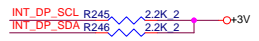


**PROJECT : Y0DD**  
 Quanta Computer Inc.

Size Custom	Document Number	Rev 1A
Block Diagram		
Date: Wednesday, January 06, 2016   Sheet 1 of 41		

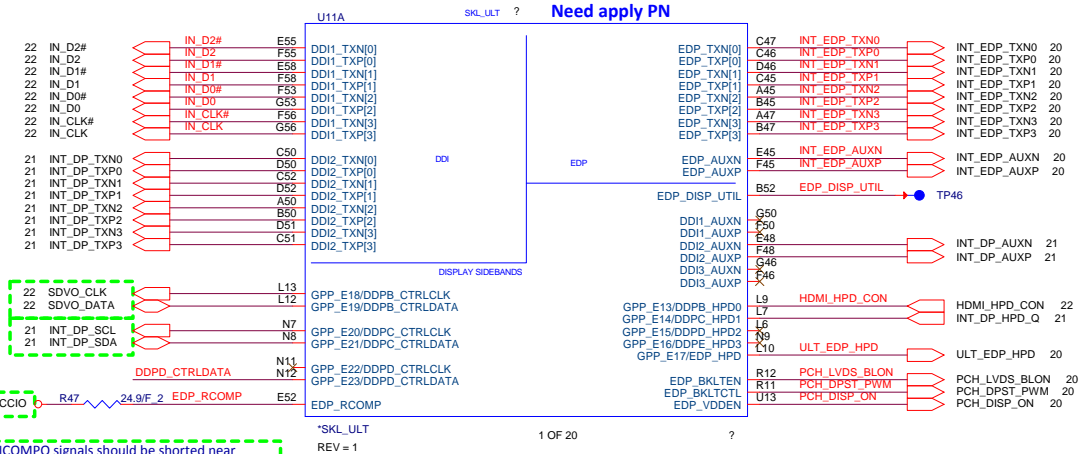
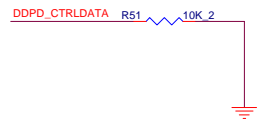
+3V 4,10,11,12,13,14,15,20,22,23,26,27,29,30,31,37,38  
+1.0V 4,6,30,36  
+VCCSTPLL 5,6,9,36,38  
+VCCIO 6,16,36

# HDMI

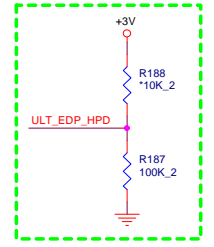


DDPB\_CTRLDATA/ GPP\_E19  
Display Port B Detected  
This signal has a weak internal pull-down.  
0 = Port B is not detected.  
1 = Port B is detected.

This signal has a weak internal pull-down.  
0 = Port C and D is not detected.  
1 = Port C and D is detected.

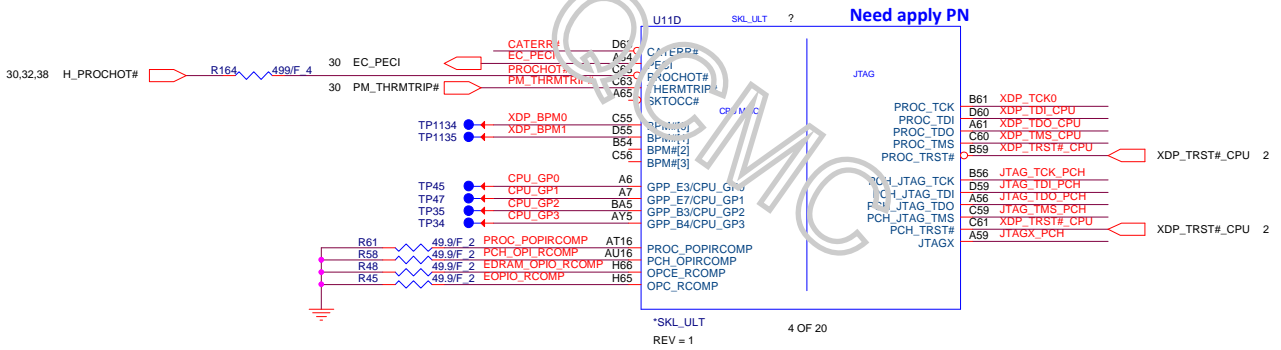
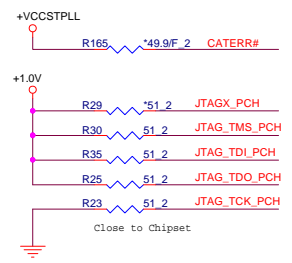


Reserve EDP\_HPD opposites circuit!

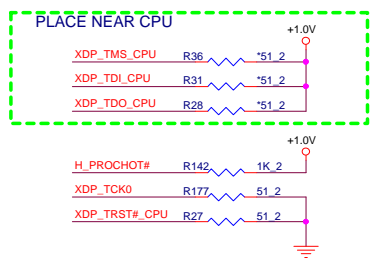



# Mini-DP

eDP\_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms



Close to EC  
Processor pull-up (CPU)  
TO BE REPLACED WITH 1K OHMS FOR SKL.  
470 OHM IS FOR I/P





**PROJECT : Y0DD**  
Quanta Computer Inc.

Size Custom	Document Number <b>SKLU (1/14)</b>	Rev 1A
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## SkyLake ULT Processor (DDR3L)

17 M\_A DQSN7-0  
17 M\_A DQSP7-0  
18 M\_B DQSN7-0  
18 M\_B DQSP7-0  
17 M\_A DQ63-0  
18 M\_B DQ63-0

+1.2VUS 6.17,18,34,36

Need apply PN

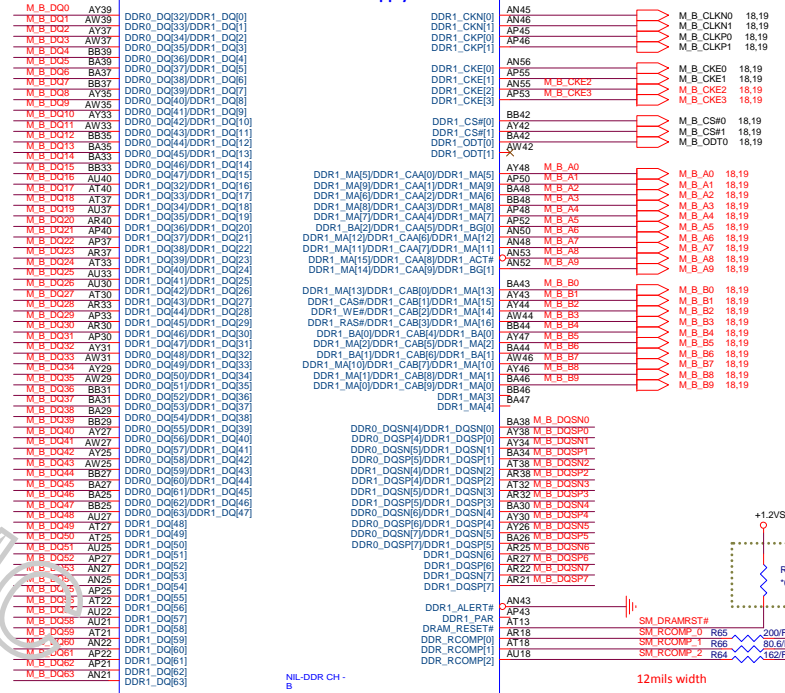


\*SKL\_ULT  
REV = 1

2 OF 20

SKL\_ULT ?

Need apply PN



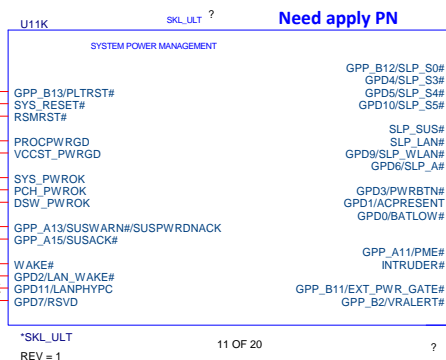
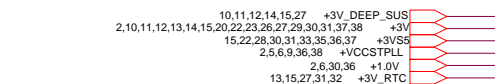
\*SKL\_ULT  
REV = 1

3 OF 20

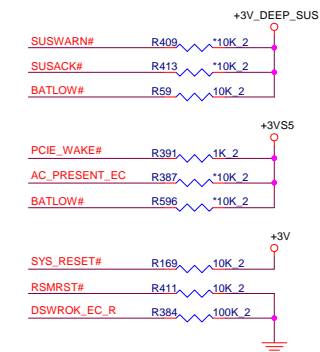


PROJECT : Y0DD  
Quanta Computer Inc.

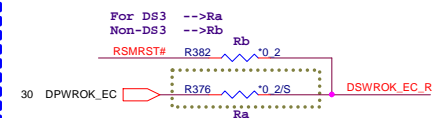
Size Custom Document Number  
SKL U (2/14)  
Date: Wednesday, January 06, 2016 Sheet 3 of 41 Rev 1A



## PCH Pull-high/low(CLG)

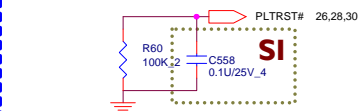


## For DS3 Sequence

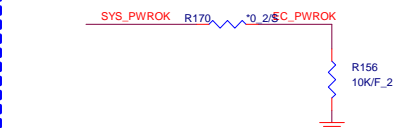
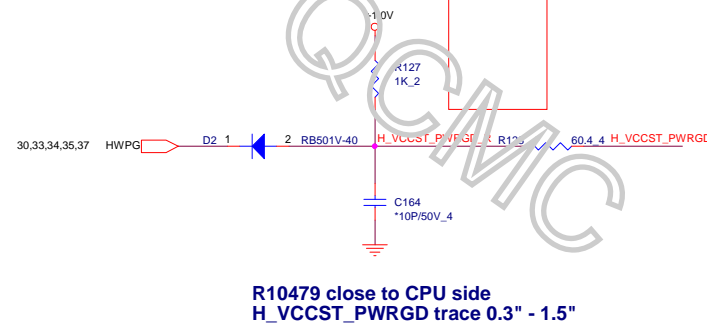
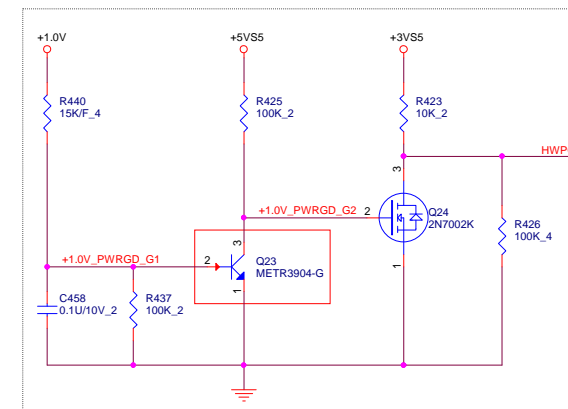


## PLTRST#(CLG)

Check Q2010 Rise/Fall time less than 100ns




## System PWR\_OK(CLG)

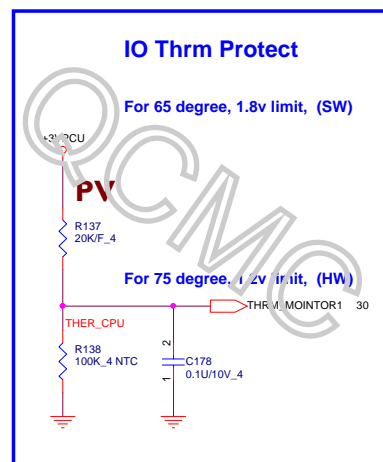
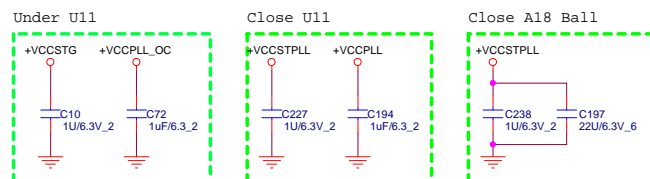
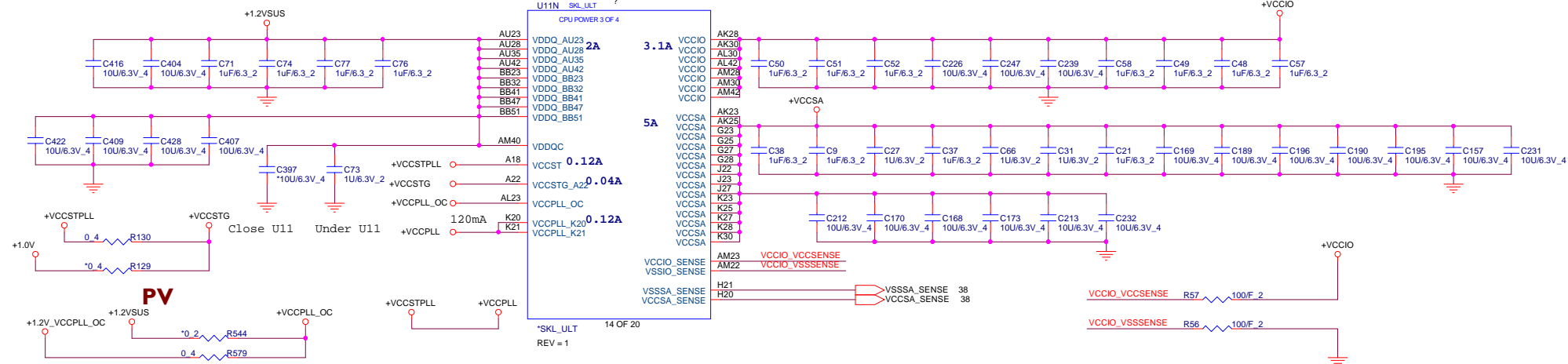
1211 Del  
+VCCSTPLL and R134R10479 close to CPU side  
H\_VCCST\_PWRGD trace 0.3" - 1.5"

1110 Add Circuit for +1.0V Power Good

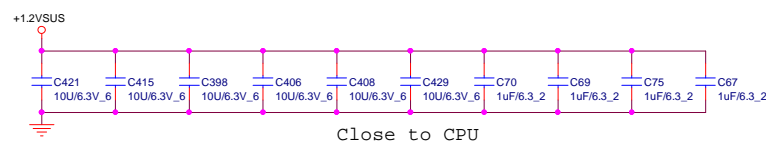
1118 Change Change Q7062 P/N from BA051440000 to  
BA039040020, Del D7002, D7003, R10526, R10527



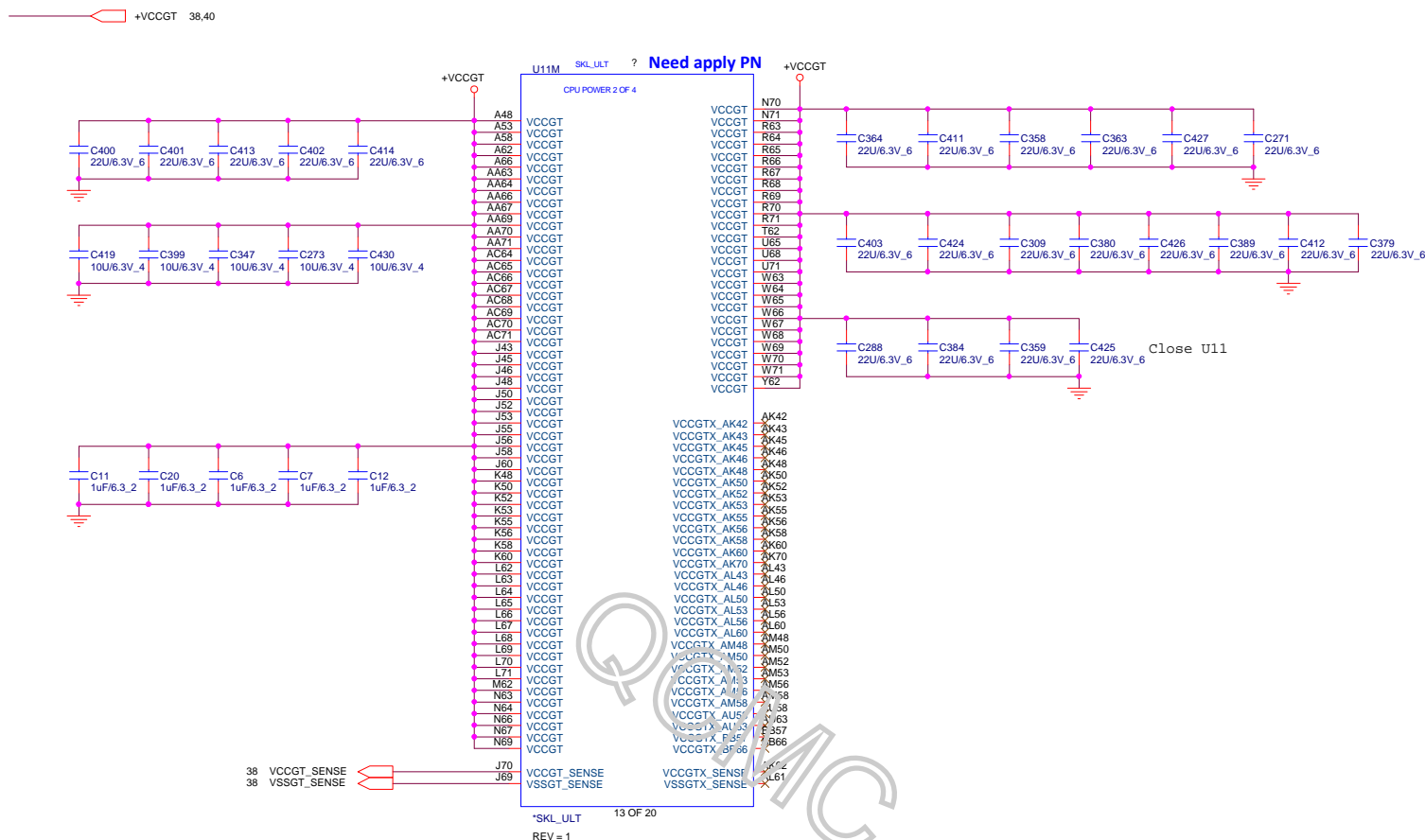
 NB5	<b>PROJECT : Y0DD</b> Quanta Computer Inc.		
	Size Custom	Document Number <b>SKL U (4/14)</b>	Rev 1A
Date: Wednesday, January 06, 2016		Sheet 5 of 41	



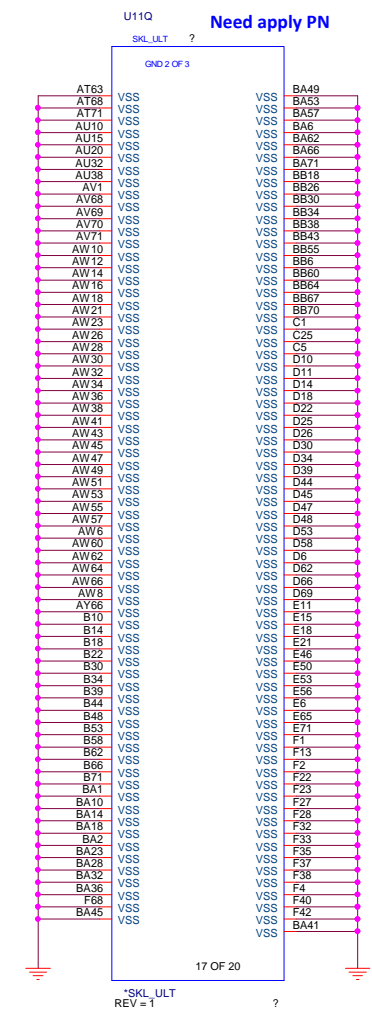
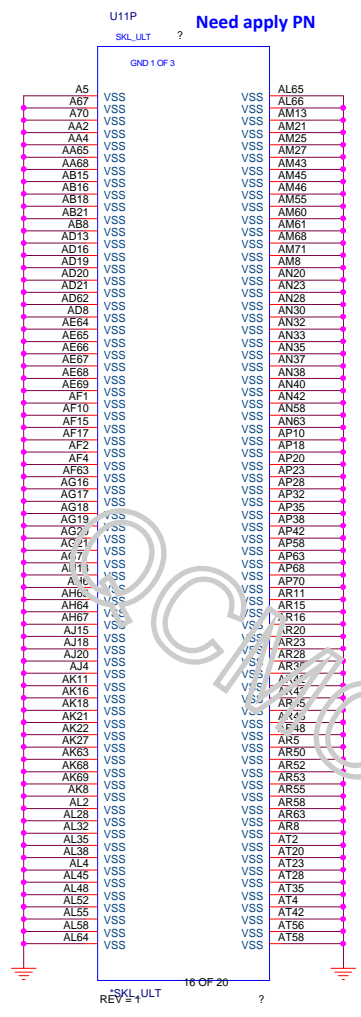
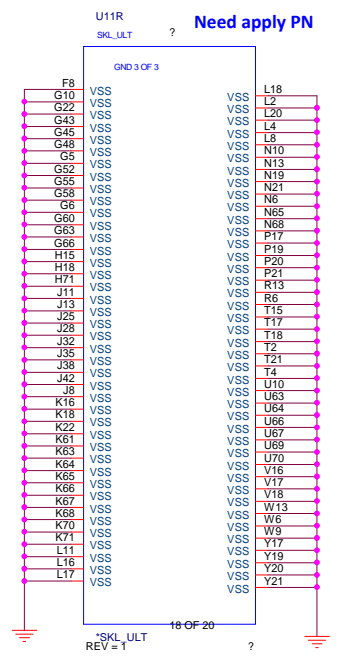
Power Rail	Description	Control
V <sub>CC</sub>	Processor IA Cores Power Rail	SVID
V <sub>CCGT</sub>	Processor Graphics Power Rails	SVID
V <sub>CCGTX</sub>	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
V <sub>CCSA</sub>	System Agent Power Rail	SVID/Fixed (SKU dependent)
V <sub>CCIO</sub>	IO Power Rail	Fixed
V <sub>CCST</sub>	Sustain Power Rail	Fixed
V <sub>CCPLL</sub>	Processor PLLs power rail	Fixed
V <sub>DDQ</sub>	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
V <sub>CCOPC</sub>	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V <sub>CCOPC_1P8</sub>	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V <sub>CCEOPIO</sub>	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed








Power Rail	Description	Control
V <sub>CC</sub>	Processor IA Cores Power Rail	SVID
V <sub>CCGT</sub>	Processor Graphics Power Rails	SVID
V <sub>CCGTX</sub>	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
V <sub>CCSA</sub>	System Agent Power Rail	SVID/Fixed (SKU dependent)
V <sub>CCIO</sub>	IO Power Rail	Fixed
V <sub>CCST</sub>	Sustain Power Rail	Fixed
V <sub>CCPLL</sub>	Processor PLLs power rail	Fixed
V <sub>DDQ</sub>	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
V <sub>CCOPC</sub>	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V <sub>CCOPC_IP8</sub>	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V <sub>CCEOPIO</sub>	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

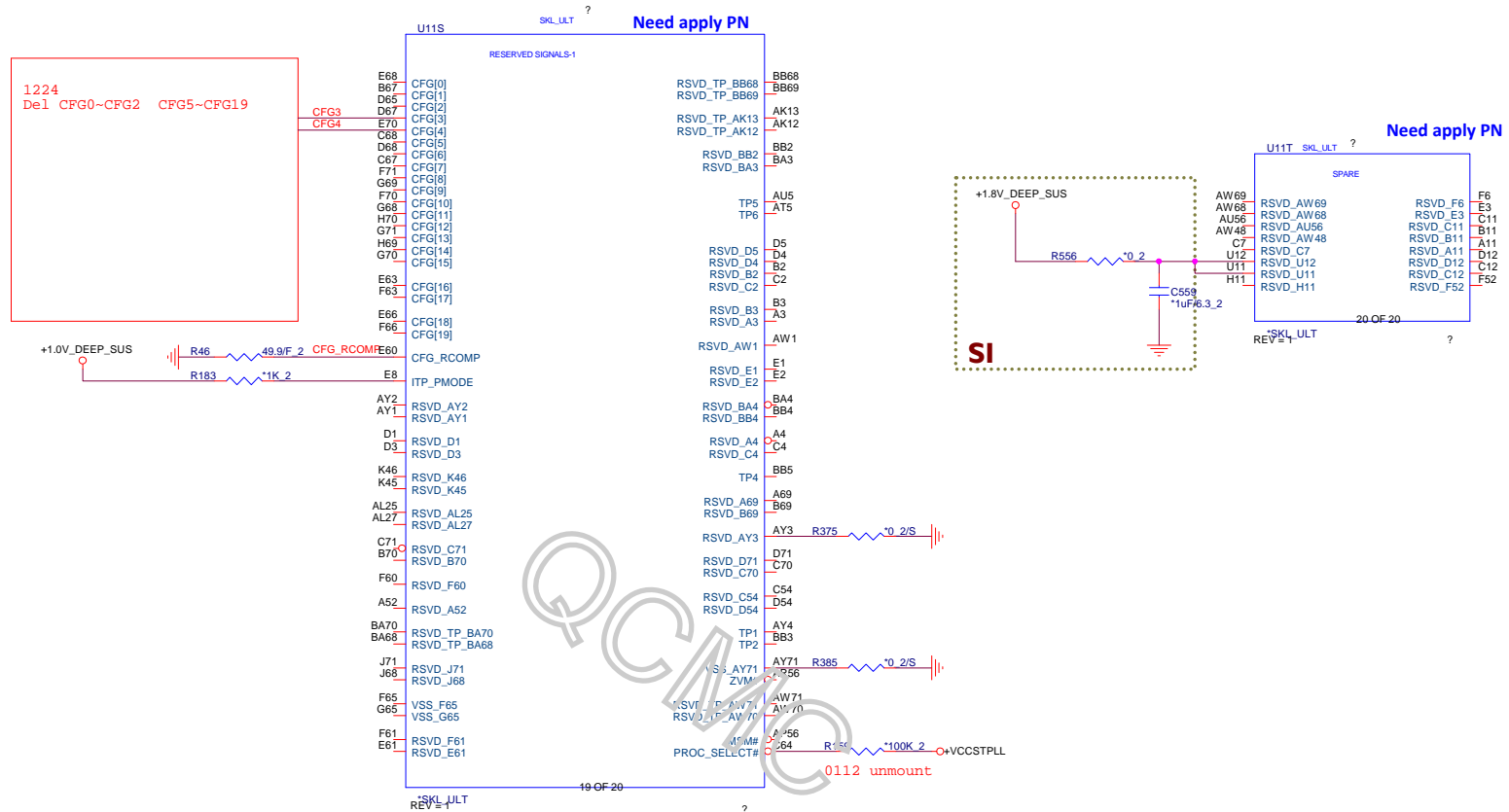




**PROJECT : Y0DD**  
Quanta Computer Inc.

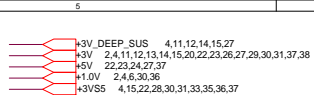
Size Custom	Document Number <b>SKL U (7/14)</b>	Rev 1A
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**Processor Strapping**

The CFG signals have a default value of '1' if not terminated on the board.

	1	0	Circuit
CFG3 (Physical Debug Enable) DFX_Privacy	Disable:	Enable: Set DFX Enable in DFX interface MSR	CFG3 R143 1K 2
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP	CFG4 R42 1K 2



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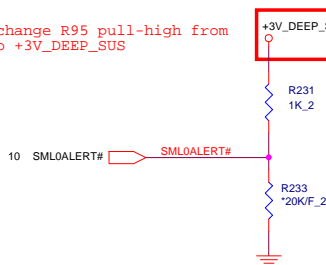
# Functional Strap Definitions

**DESIGN NOTE:**  
WEAK PULL UP RESISTOR PRESENT ON THIS NET

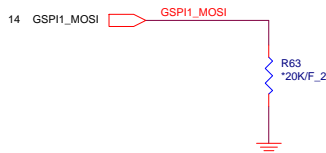


**TOP SWAP OVERRIDE**  
HIGH - TOP SWAP ENABLE  
LOW-DISABLED  
HIGH: LPC SELECTED FOR SYSTEM FLASH  
WEAK INTERNAL PD

1212 change R95 pull-high from +3V to +3V\_DEEP\_SUS



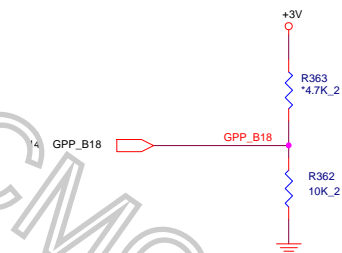
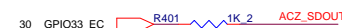
**No Boot:**  
The signal has a weak internal pull-down.  
0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality).  
1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS.



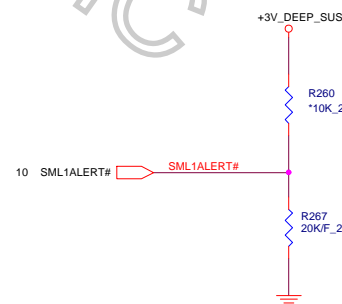
**No Boot:**  
The signal has a weak internal pull-down.  
This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Chipset Configuration Registers: Offset 3410h:Bit 10). This strap is used in conjunction with Boot BIOS Destination Selection 0 strap.  
Bit 10      Boot BIOS Destination  
0            SPI  
1            LPC



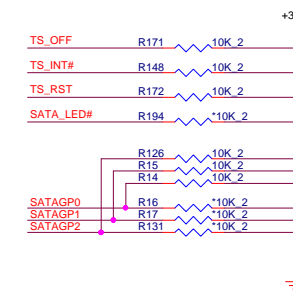
**No Boot:**  
The signal has a weak internal pull-down.  
0 = Enable security measures defined in the Flash Descriptor.  
1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY. This function is useful when running ITP/XDP.



**No Boot:**  
The signal has a weak internal pull-down.  
0 = Disable No Reboot mode.  
1 = Enable No Reboot mode (PCH will disable the TCO Timer system reboot feature).  
This function is useful when running ITP/XDP.



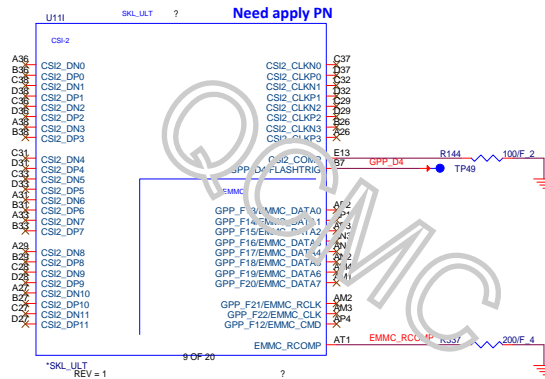
**No Boot:**  
The signal has a weak internal pull-down.  
0 = LPC is selected for EC.  
1 = eSPI is selected for EC.



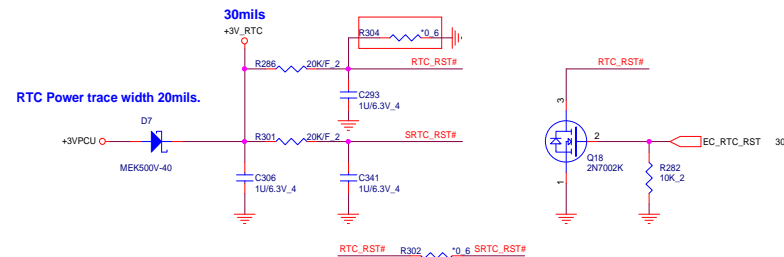
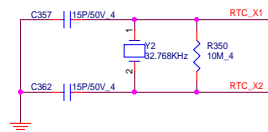
## USB2.0 Port Mapping Table

USB2.0	Function
PORT-1	USB3.0 MB-1
PORT-2	USB3.0 MB-2
PORT-3	USB3.0 MB-3
PORT-4	Sensor Hub
PORT-5	NC
PORT-6	Camera
PORT-7	WLAN
PORT-8	Touch Screen
PORT-9	NC
PORT-10	NC



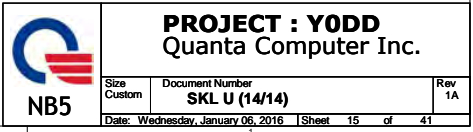


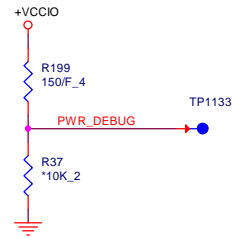

 +3V<sub>RTC</sub>    4,15,27,31,32  
 +3V<sub>PCU</sub>    6,15,27,28,30,31,32,33






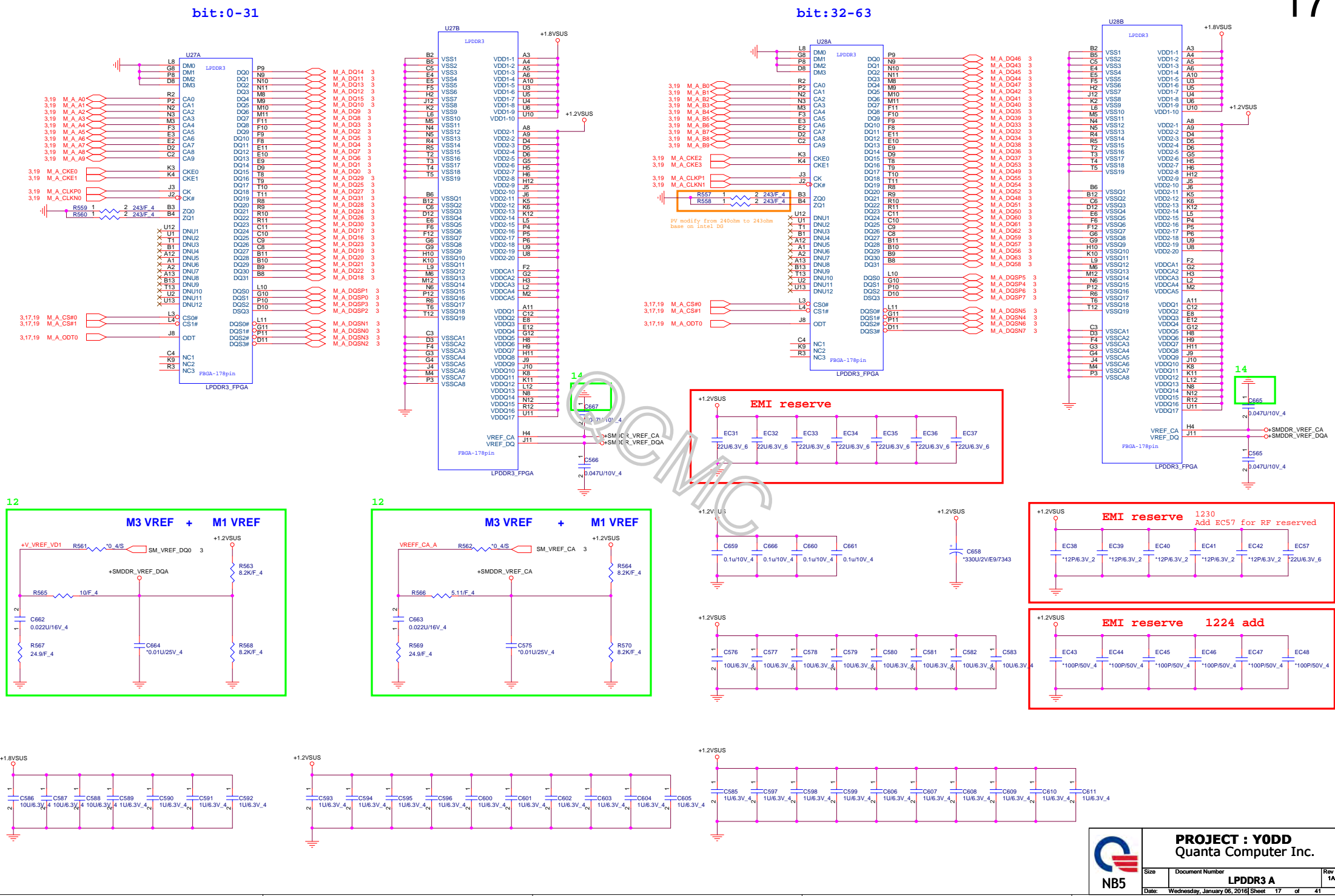




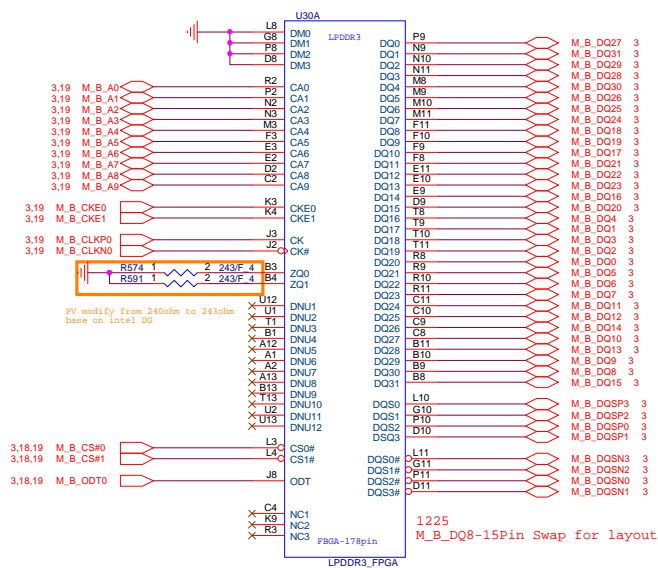


QCMC

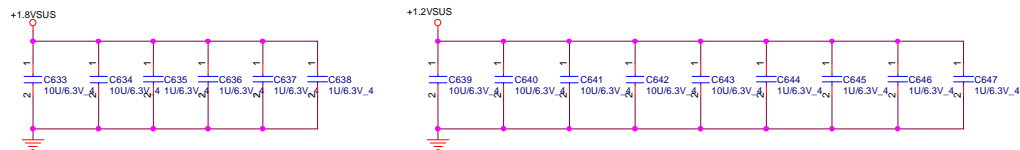
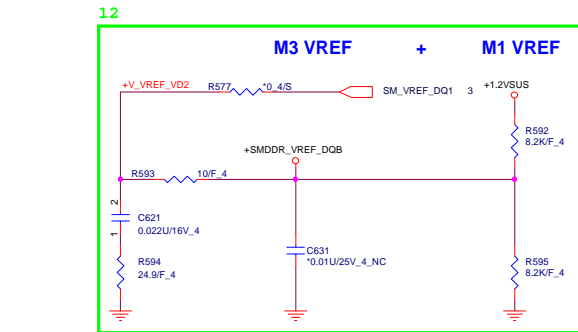
 <b>PROJECT : Y0DD</b> Quanta Computer Inc.		
Size Custom	Document Number <b>XDP/APS</b>	Rev 1A
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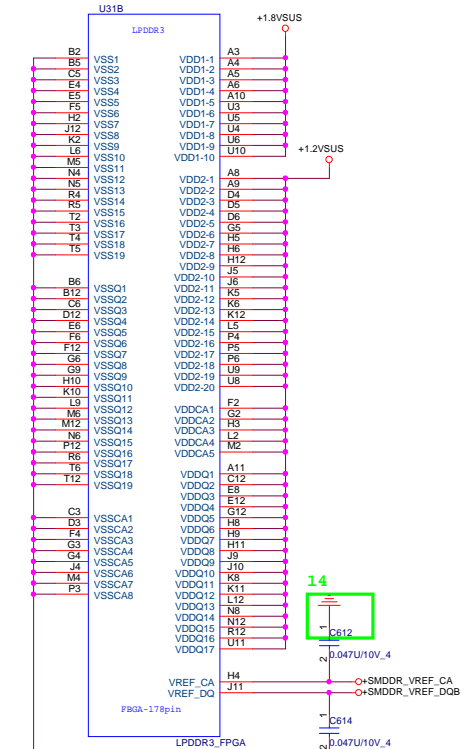
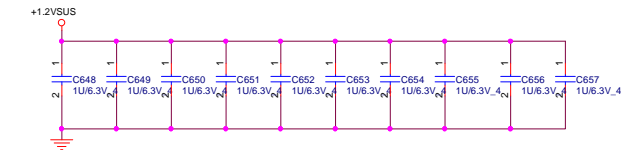
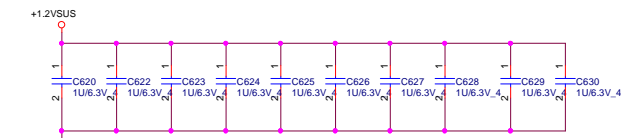
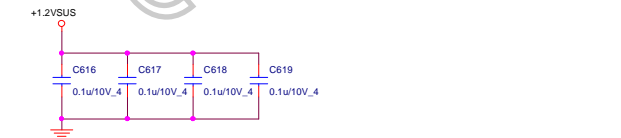
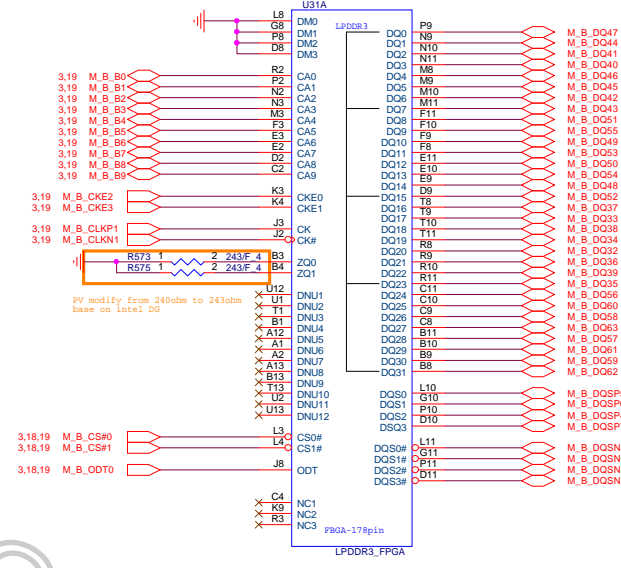
bit:0-31



1225  
M\_B\_DQ8-15Pin Swap for layout

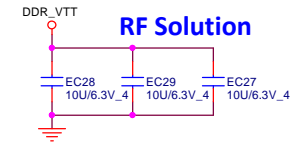
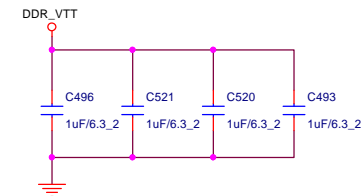
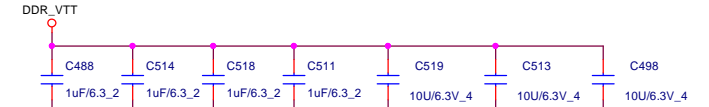
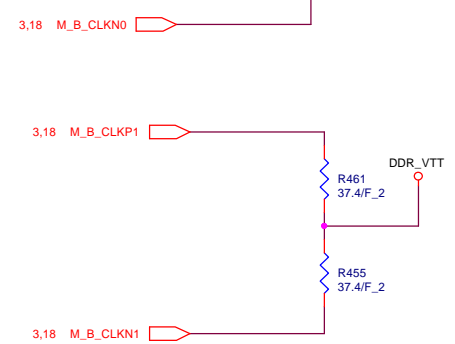
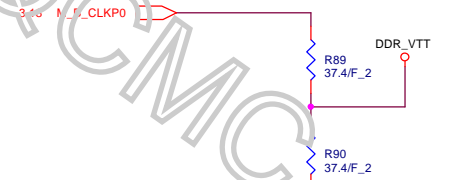
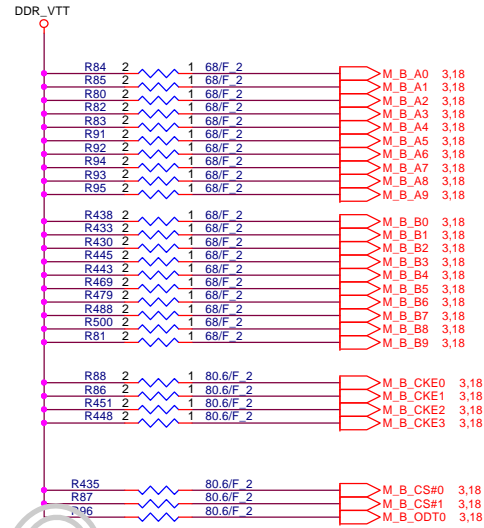
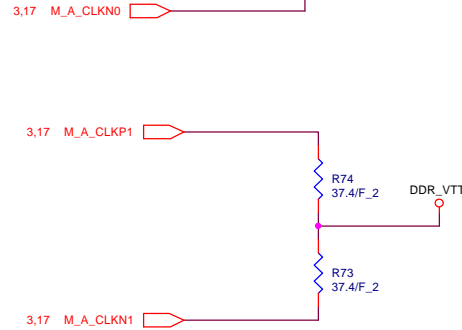
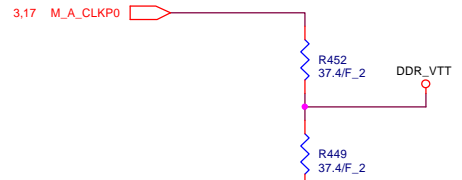
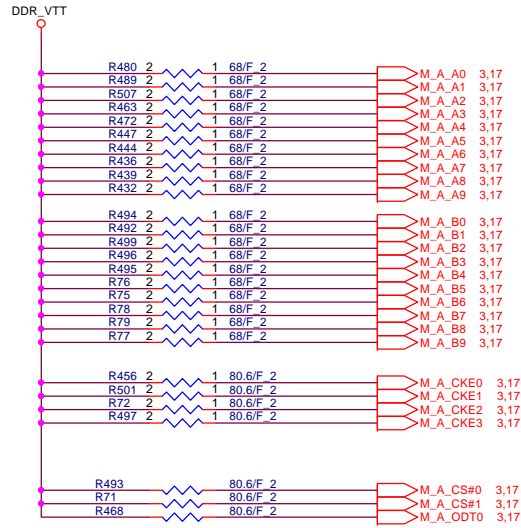


bit:32-63



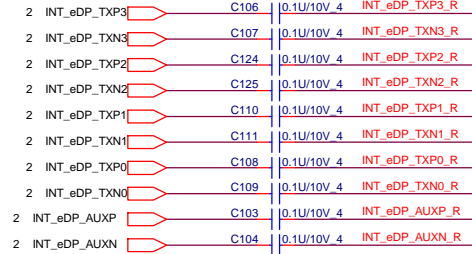
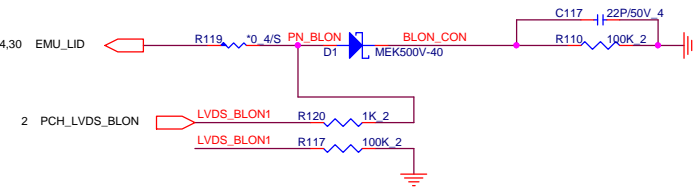
**PROJECT : Pegasus**  
**Quanta Computer Inc.**

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	<b>LPDDR3 B</b>	
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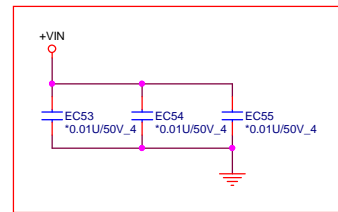


**PROJECT : YODD**  
 Quanta Computer Inc.

Size Custom	Document Number <b>LPDDR3 TERMINATION</b>	Rev 1A
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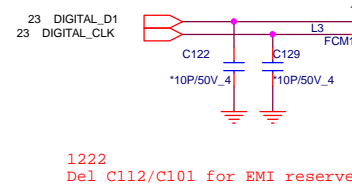
Add EC53, EC54, EC55 for EMI



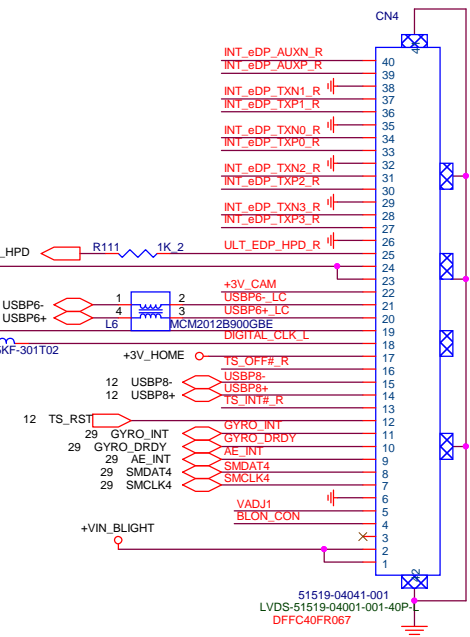
100mA +VIN\_BRIGHT

1222 Del L28/L29 for OLED reserve

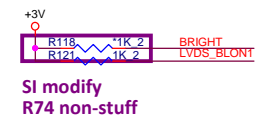
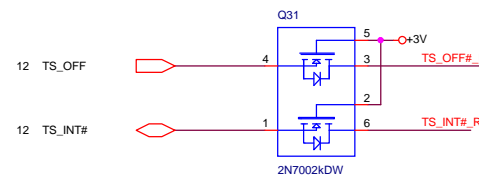
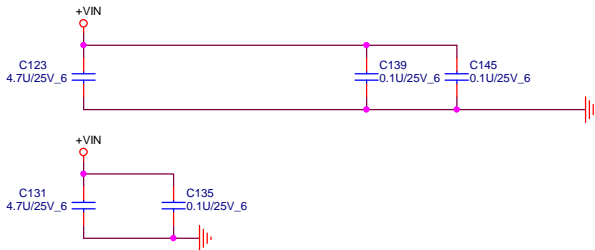
1225 L6 Pin Swap for layout



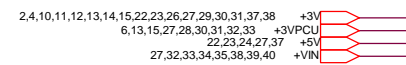
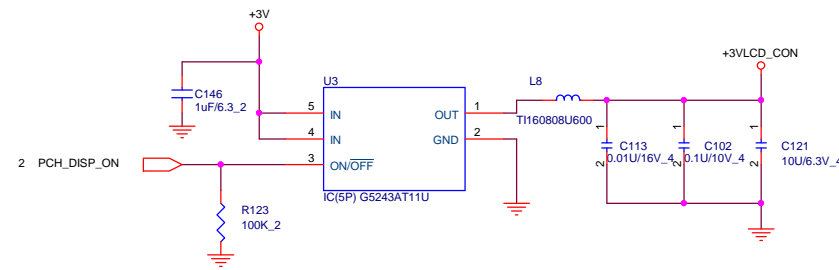
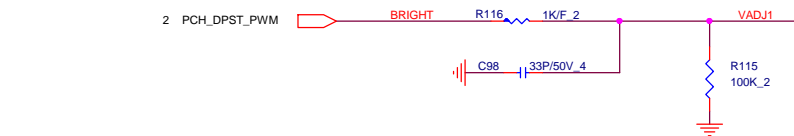
1222 Del C112/C101 for EMI reserve



51519-04041-001  
LVDS-51519-04001-001-40P  
DFFC40FR067



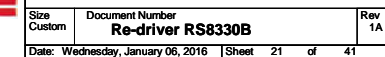
SI modify  
R74 non-stuff



**PROJECT : YODD**  
Quanta Computer Inc.

Size Custom	Document Number <b>LCD CONN/CAM/LID</b>	Rev 1A
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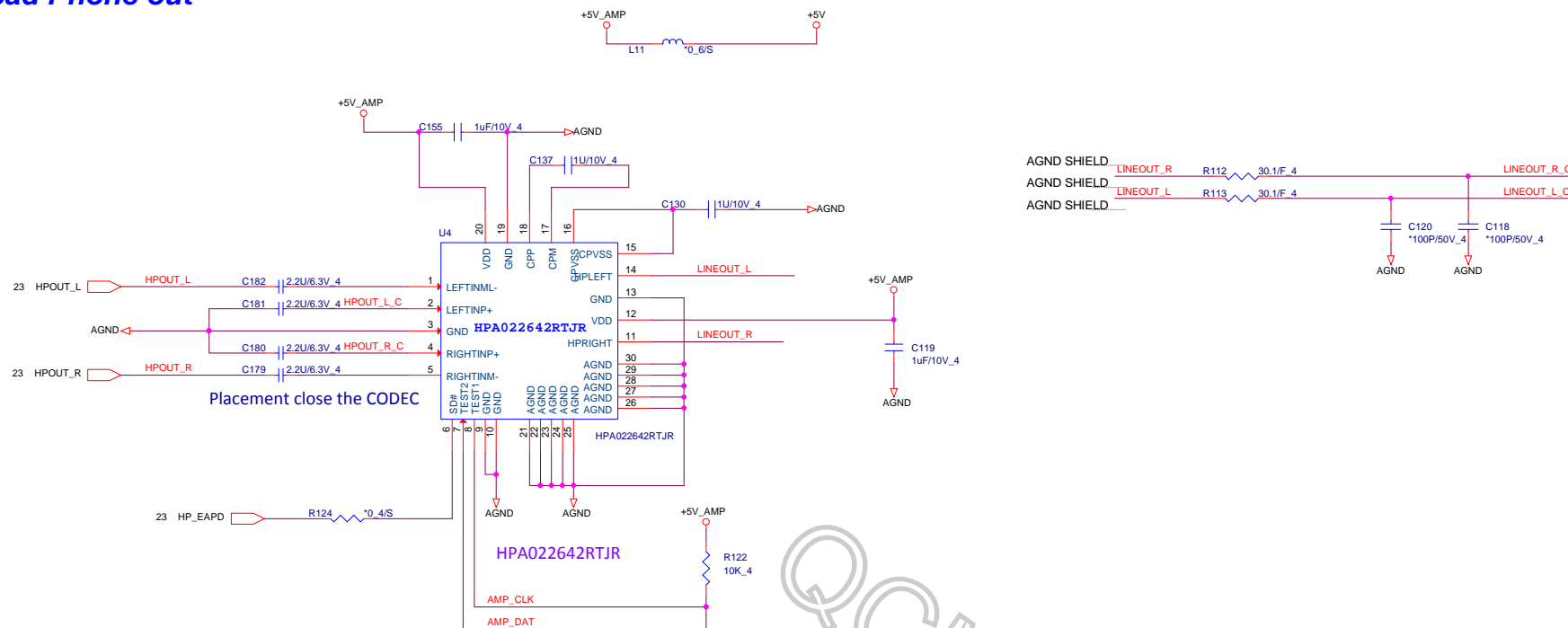








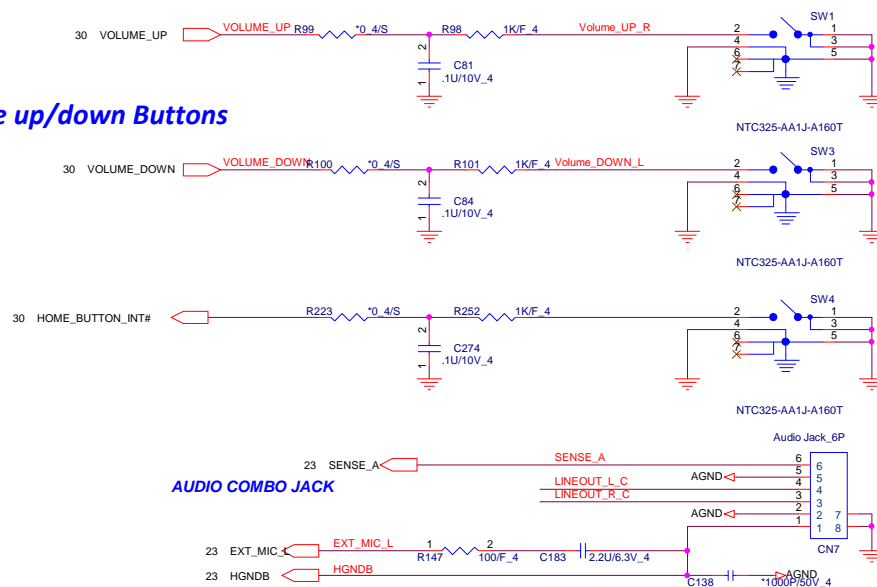
## Head Phone out



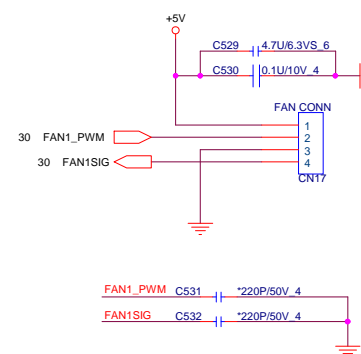
## Audio combo JACK &amp; Volume up/down Button

FAN

## Volume up/down Buttons



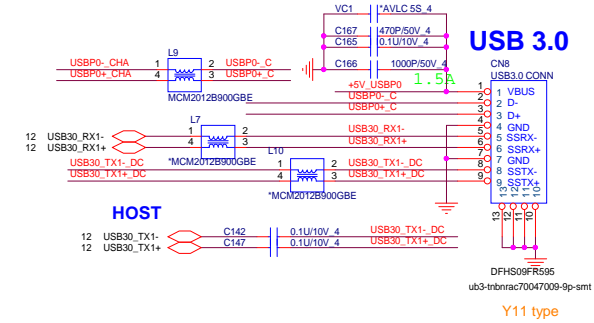
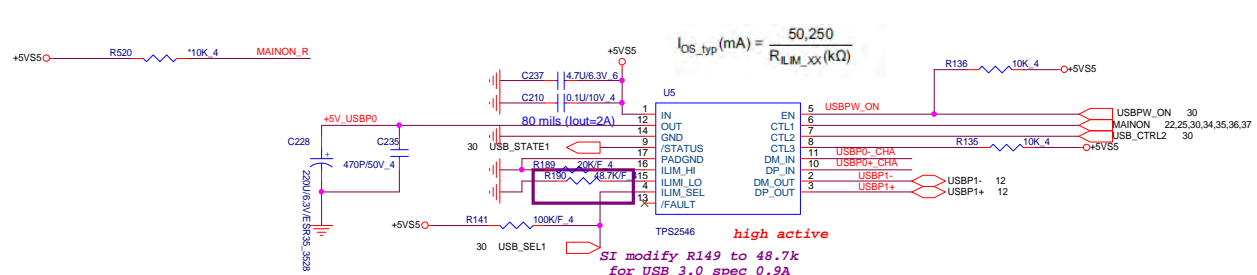
1203  
Update footprint from 88266-0400-4p-1 to 88266-04x1-4p-1-sm



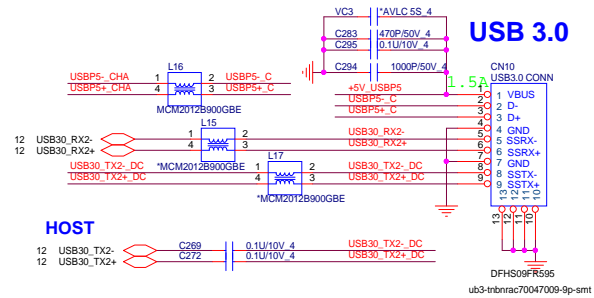
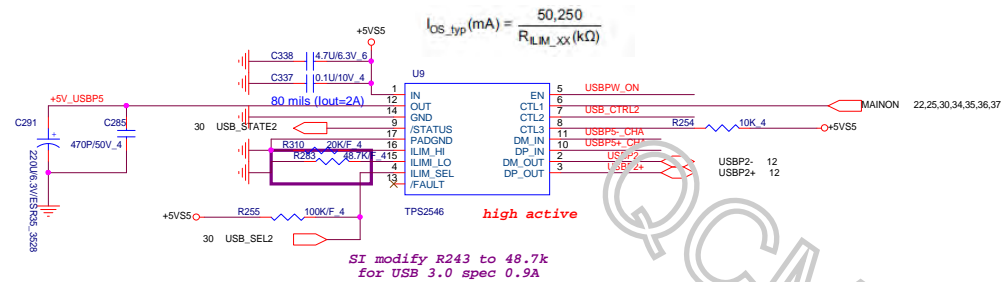
2,4,10,11,12,13,14,15,20,22,23,26,27,29,30,31,37,38 +3V  
22,23,27,37 +5V  
4,25,33,34,35,36,37,38,39,40 +5VSS

	<b>PROJECT : YODD</b>		
	Quanta Computer Inc.		
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	<b>AUDIO AMP</b>		
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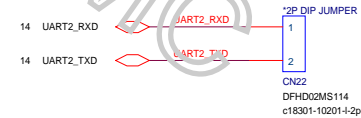
PV ADD R554/R555/R556 10k for USB 3.0 PU



1203  
Update footprint from ub3-tbnbrac70047009-9p to ub3-tbnbrac70047009-9p-smt



UART



Left side USB 2.0/3.0 Combo

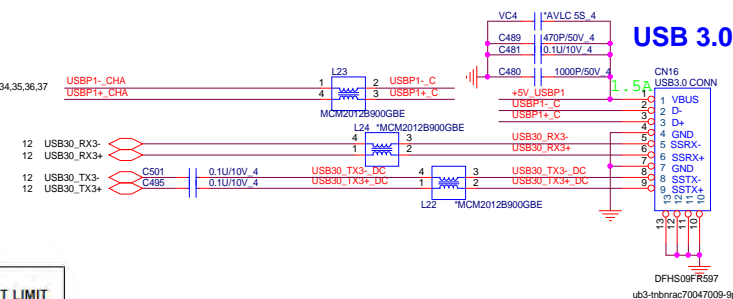
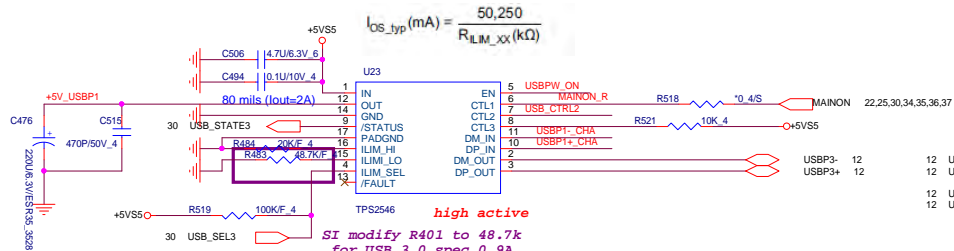


Table 3. Control Pin Settings Matched to System Power States

SYSTEM GLOBAL POWER STATE	TPS2546 CHARGING MODE	CTL1	CTL2	CTL3	ILIM_SEL	CURRENT LIMIT SETTING
S0	SDP1	1	1	0	1 or 0	ILIM_HI / ILIM_LO
S0	SDP2, no discharge to / from CDP	1	1	1	0	ILIM_LO
S0	CDP, load detection with ILIM_LO + 60mA thresholds or if a BC1.2 primary detection occurs	1	1	1	1	ILIM_HI
S4/S5	Auto mode, load detection with power wake thresholds	0	0	1	1	ILIM_HI
S3/S4/S5	Auto mode, no load detection	0	0	1	0	ILIM_HI
S3	Auto mode, keyboard/mouse wake up, load detection with ILIM_LO + 60 mA thresholds	0	1	1	1	ILIM_HI
S3	Auto mode, keyboard/mouse wake-up, no load detection	0	1	1	0	ILIM_HI
S3	SDP1, keyboard/mouse wake-up	0	1	0	1 or 0	ILIM_HI / ILIM_LO

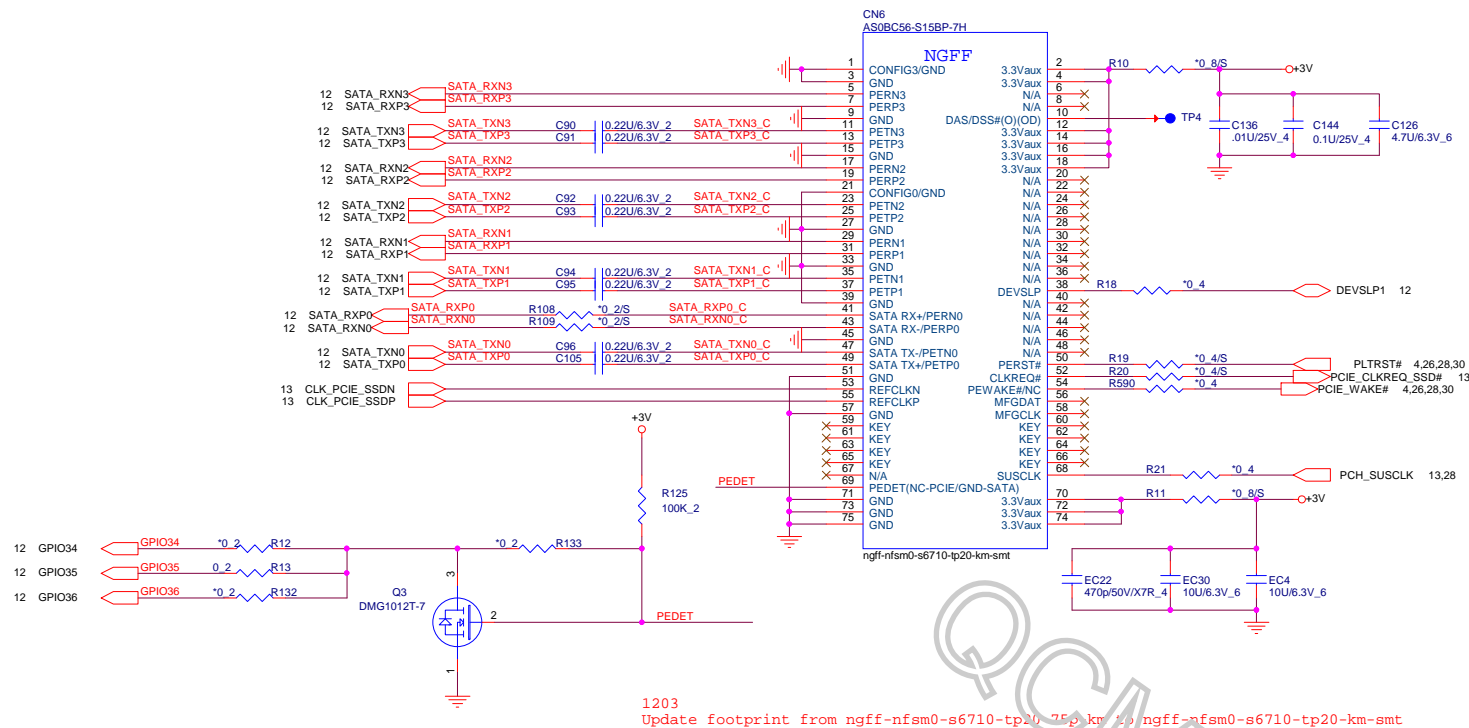
4,15,22,28,30,31,33,35,36,37  
4,33,34,35,36,37,38,39,40  
6,13,15,27,28,30,31,32,33

+5VSS  
+5VSS  
+3VPCU

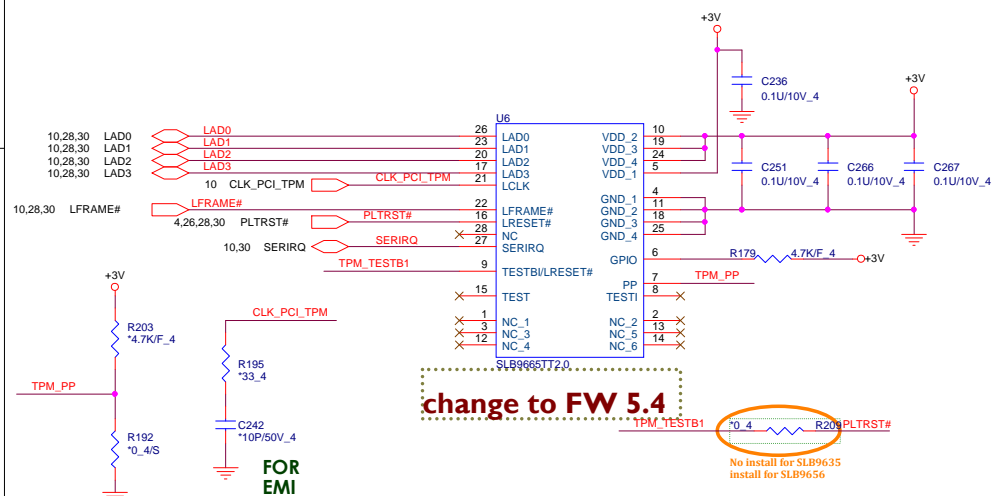


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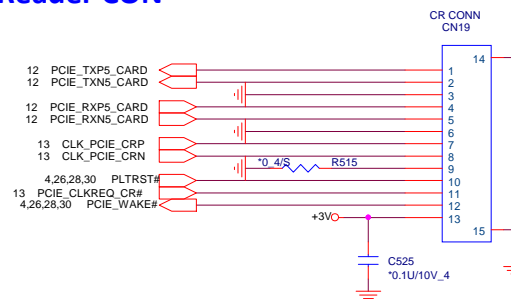
Size Custom Document Number USB20/30 Rev 1A  
Date: Wednesday, January 06, 2016 1 Sheet 25 of 41



## TPM (2.0)



## Card Reader CON



2,4,10,11,12,13,14,15,20,22,23,27,29,30,31,37,38 +3V  
22,23,24,27,37 +5V  
6,13,15,27,28,30,31,32,33 +3VPCU

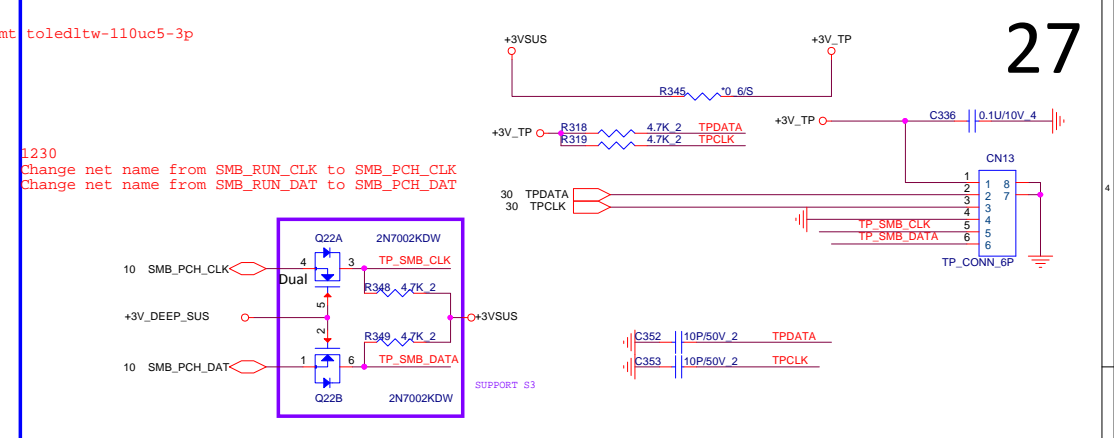
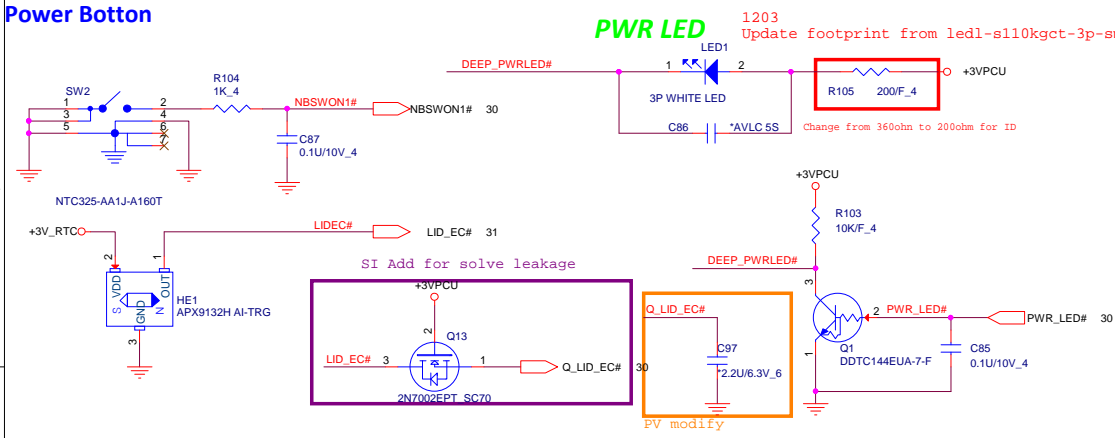


**PROJECT : YODD**  
**Quanta Computer Inc.**

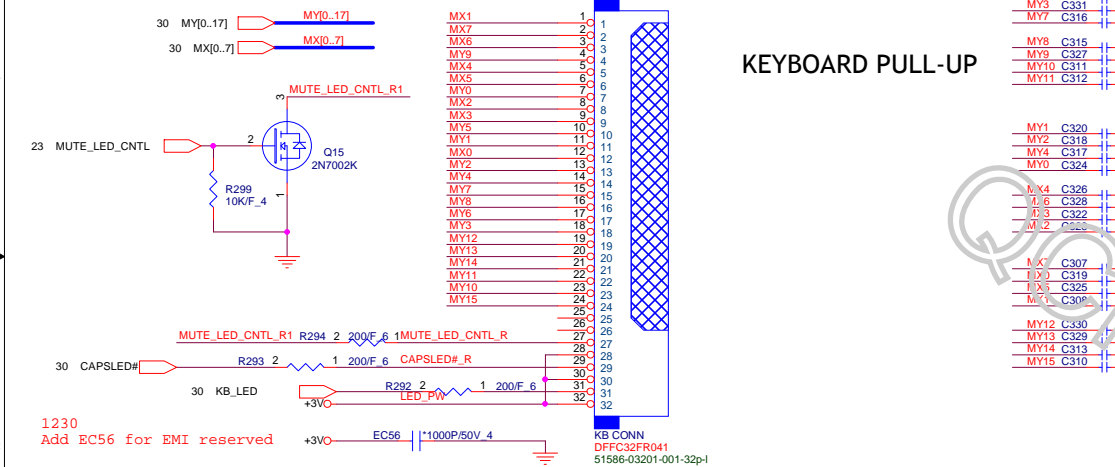
Size Custom	Document Number <b>NGFF HDD/TPM/CR</b>	Rev 1A
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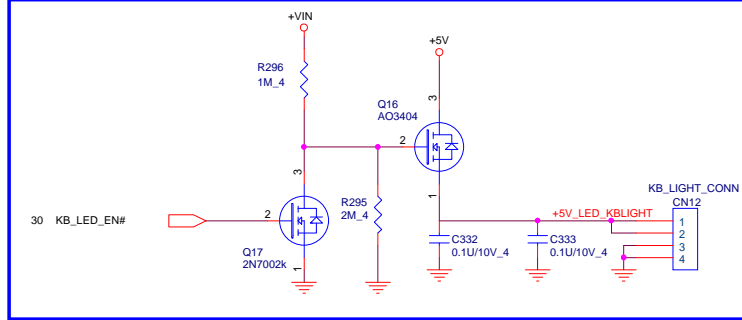
# Power Button



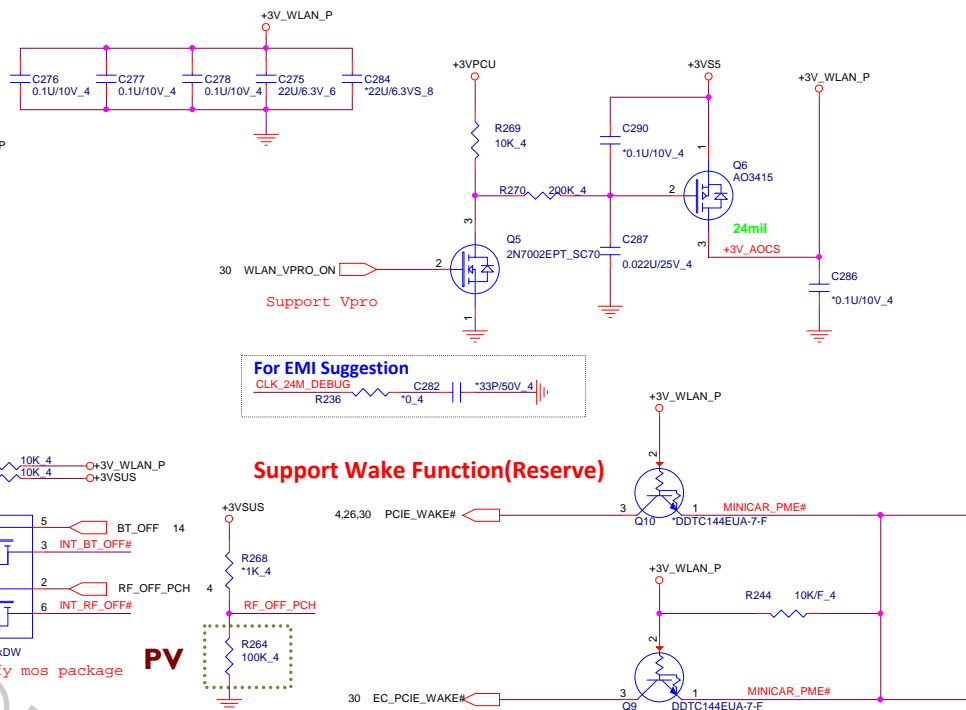
## KEYBOARD Con.



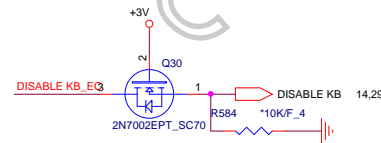
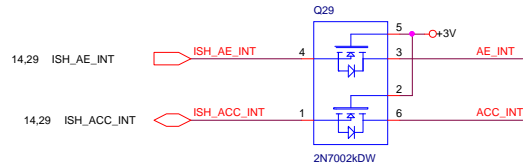
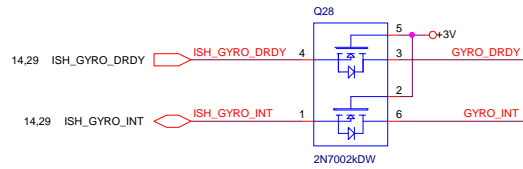
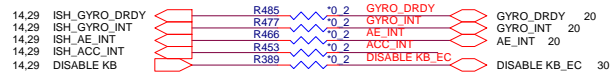
## KB backlight



2,4,10,11,12,13,14,15,20,22,23,26,29,30,31,37,38 +3V  
22,23,24,37 +5V  
6,13,15,28,30,31,32,33 +3VPCU

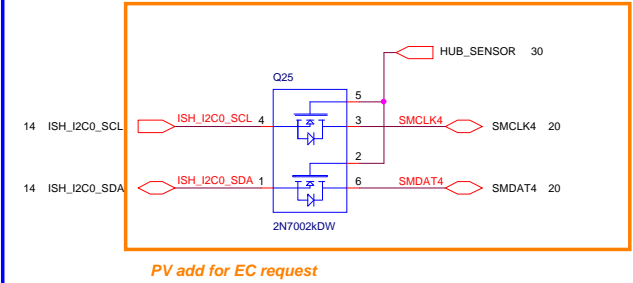
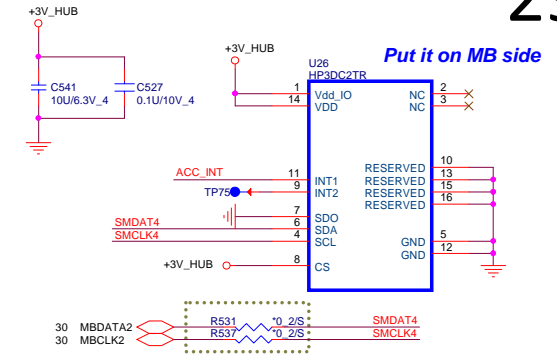


**WWW.AliSaler.Com**

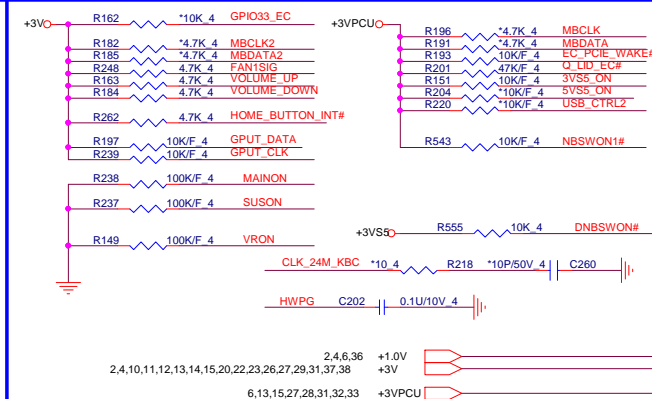
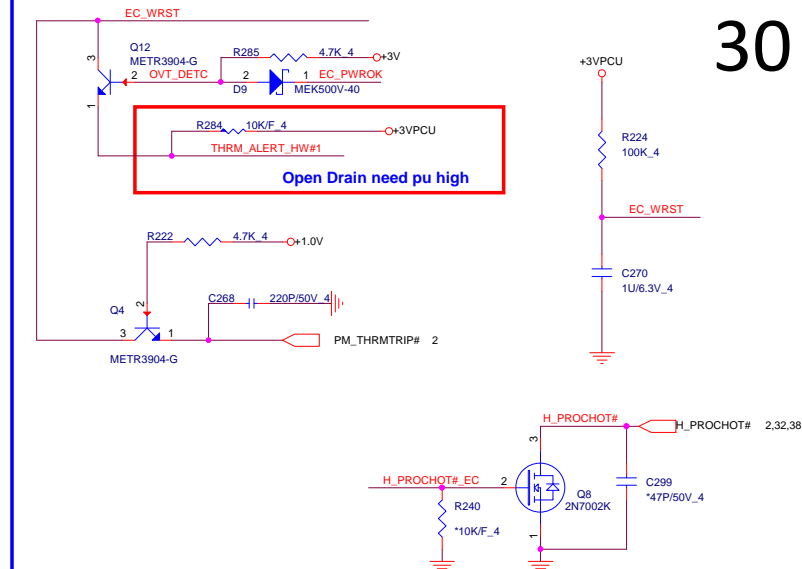
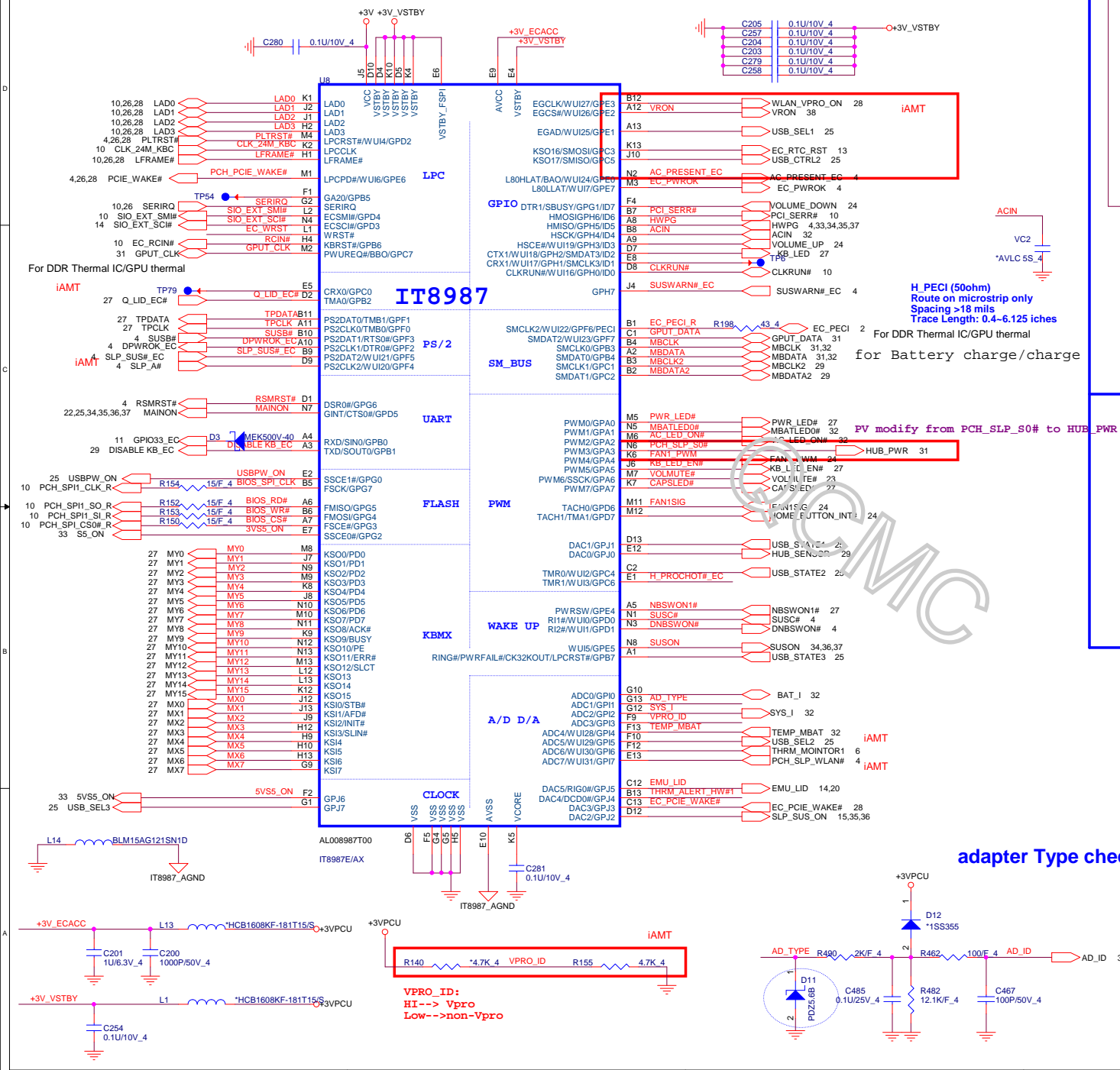


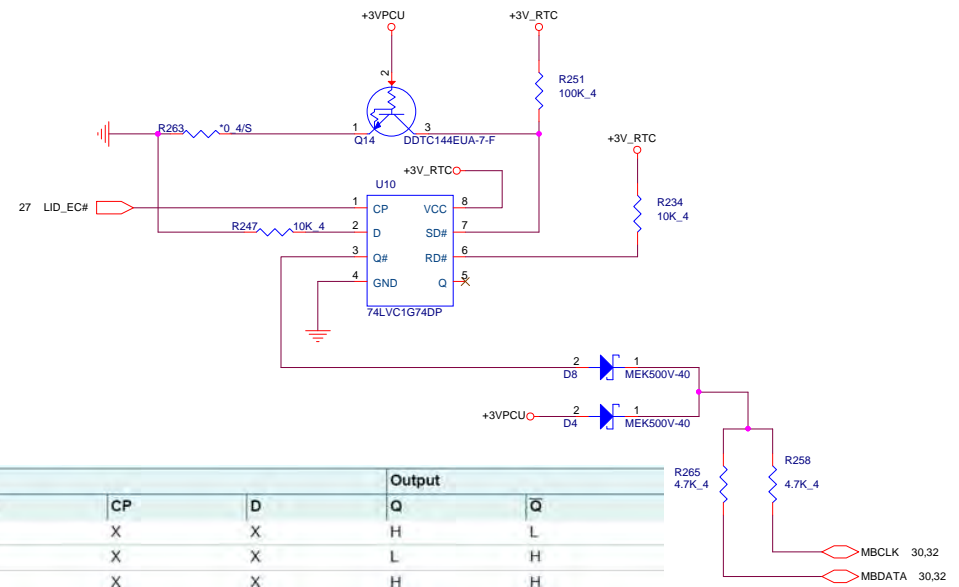
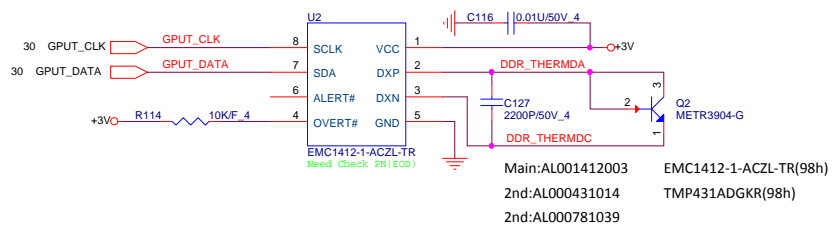
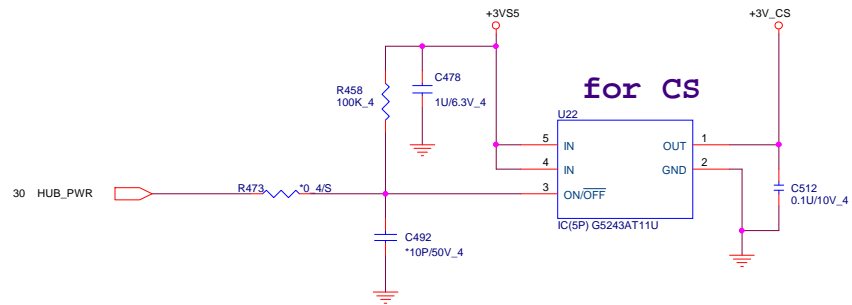
## Accelerometer Sensor

29



1222  
Del Q26/ R587/ R588 for OLED reserve



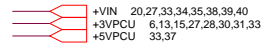


Input				Output	
SD	RD	CP	D	Q	Q̄
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H

[1] H = HIGH voltage level;  
L = LOW voltage level;  
X = don't care.

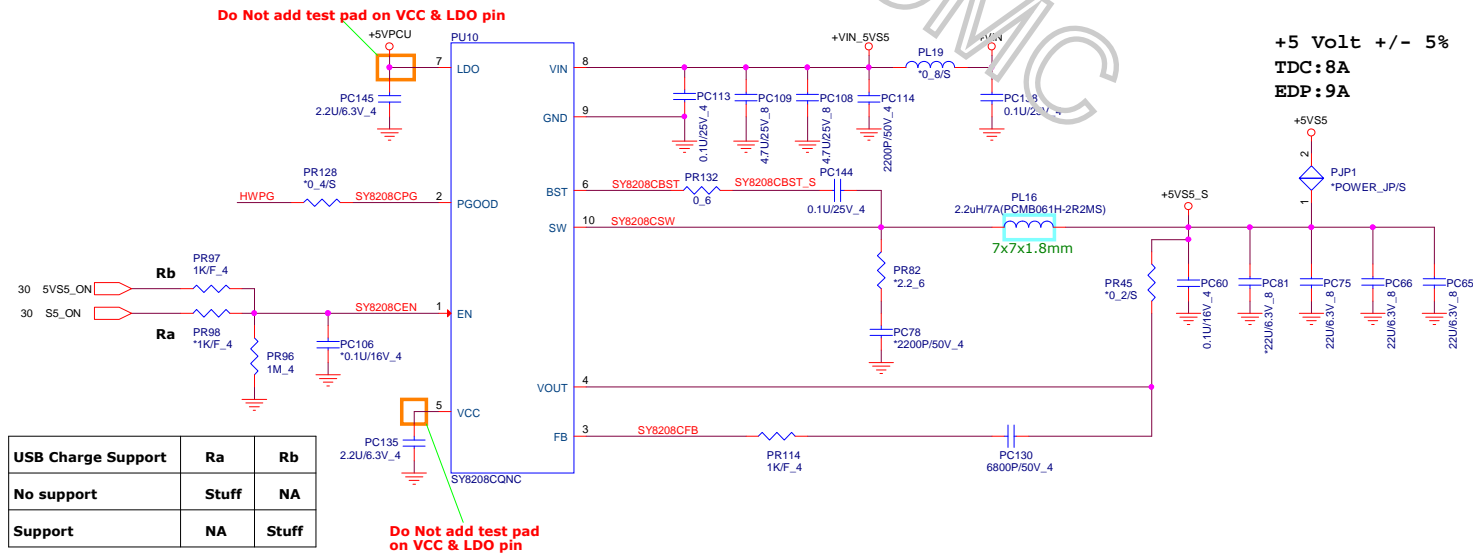
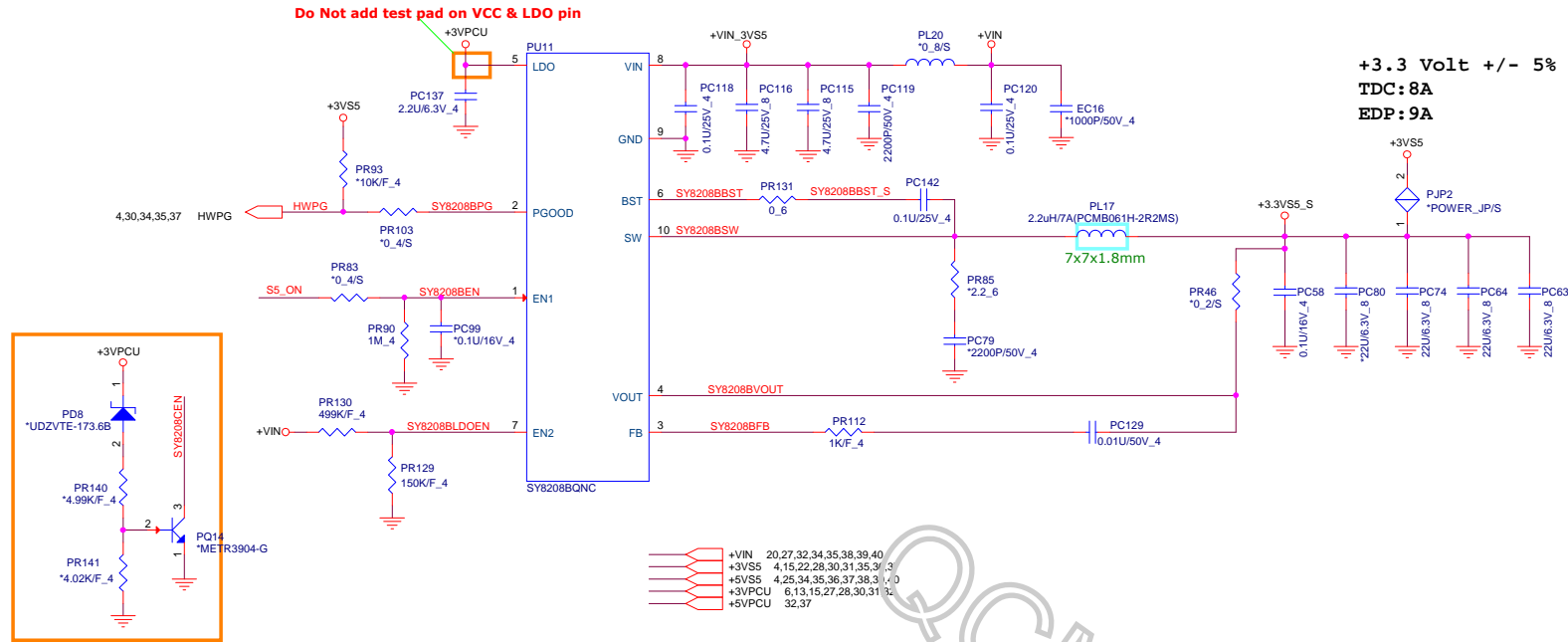
Input				Output	
SD	RD	CP	D	Q <sub>n+1</sub>	Q̄ <sub>n+1</sub>
H	H	↑	L	L	H
H	H	↑	H	H	L

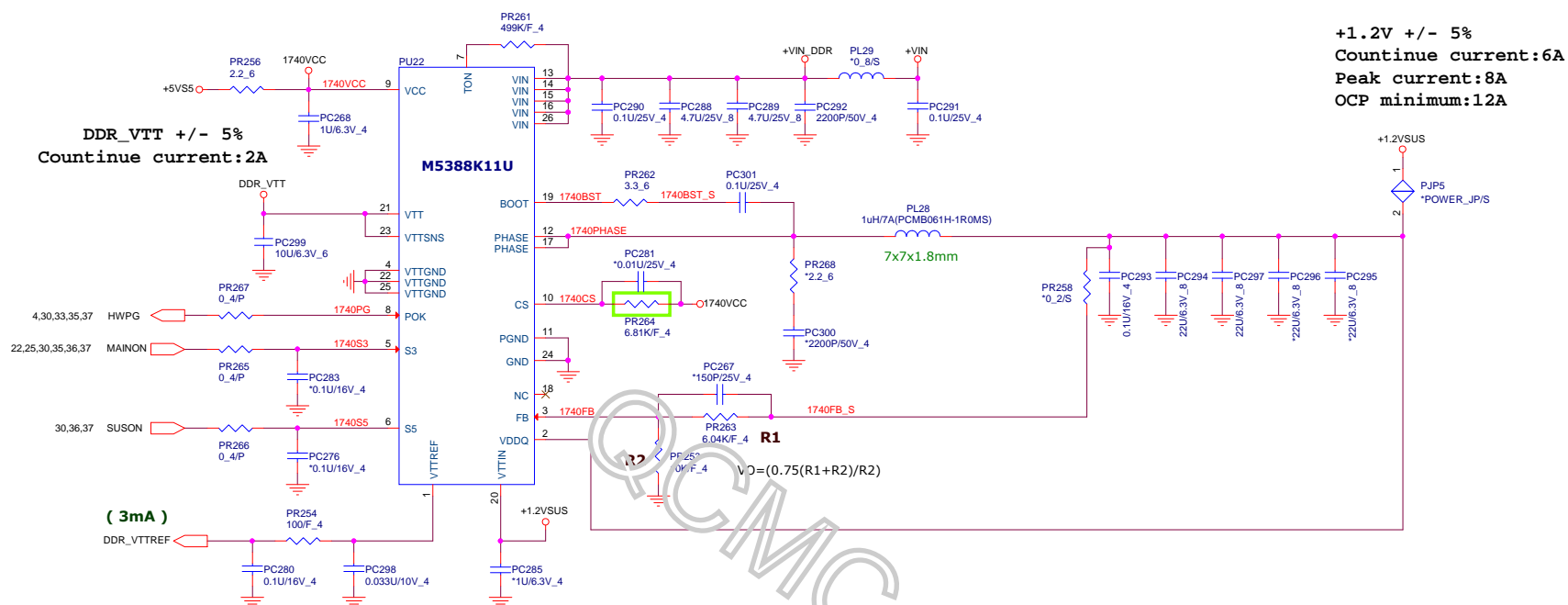
[1] H = HIGH voltage level;  
L = LOW voltage level;  
↑ = LOW-to-HIGH CP transition;  
Q<sub>n+1</sub> = state after the next LOW-to-HIGH CP transition.



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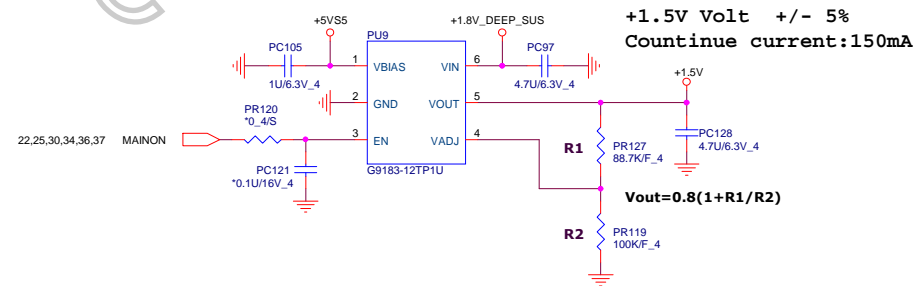
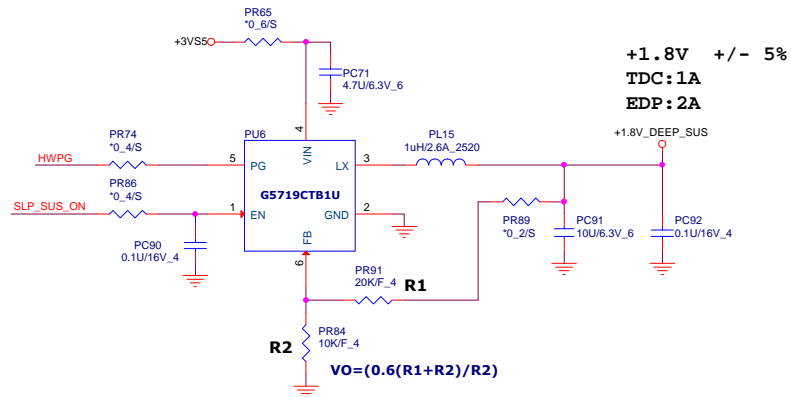
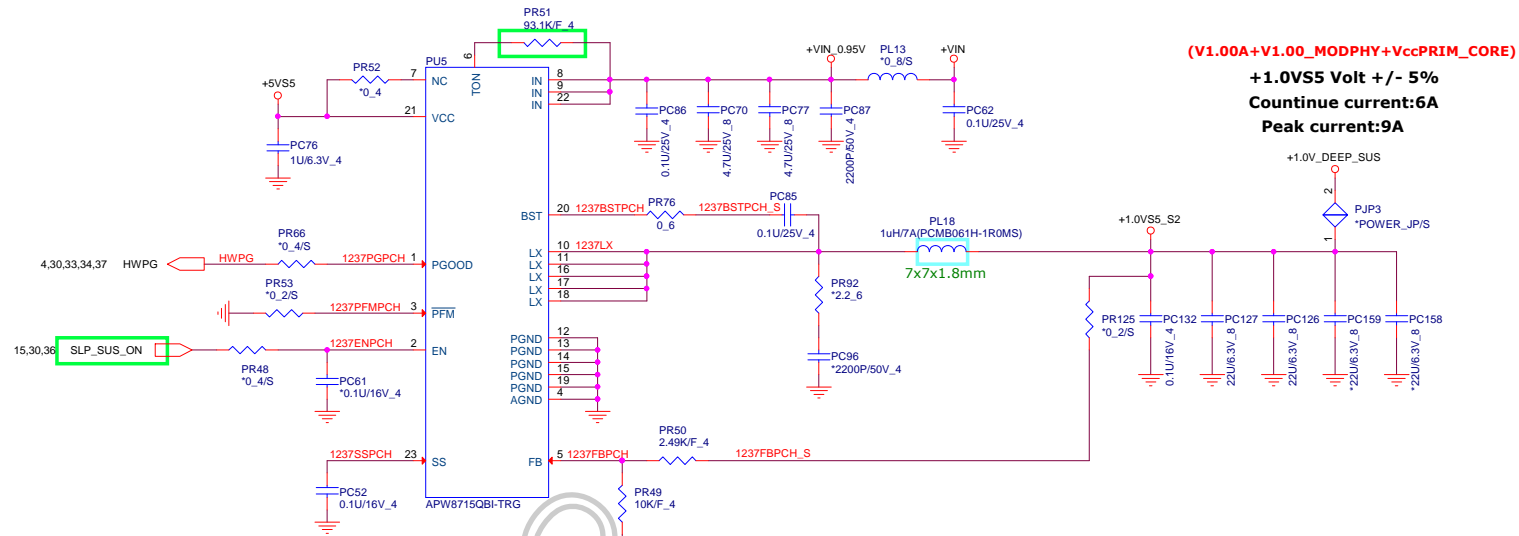






	S3	S5	+1.2VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3 (mainon off)	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

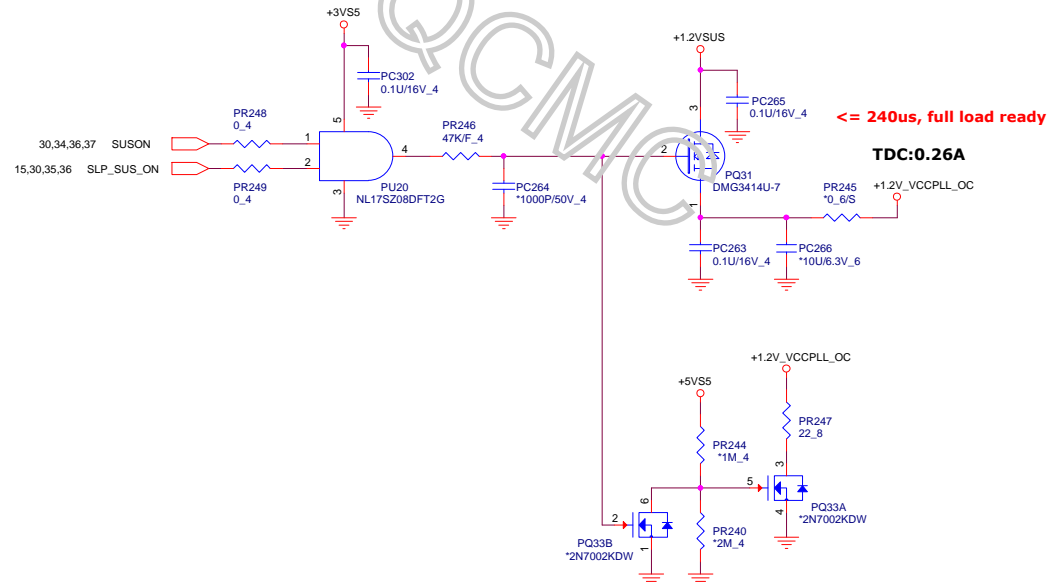
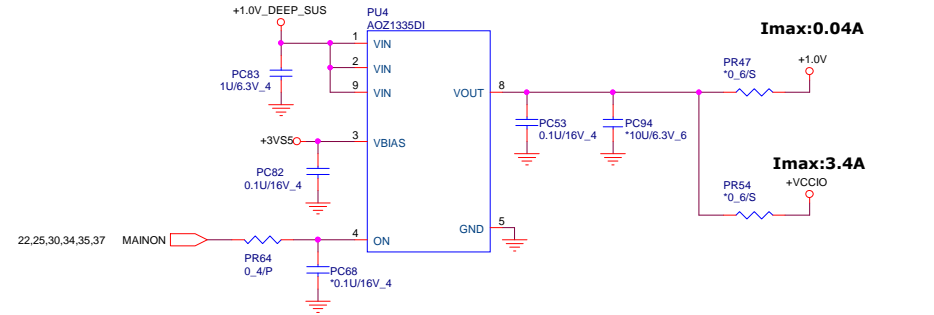
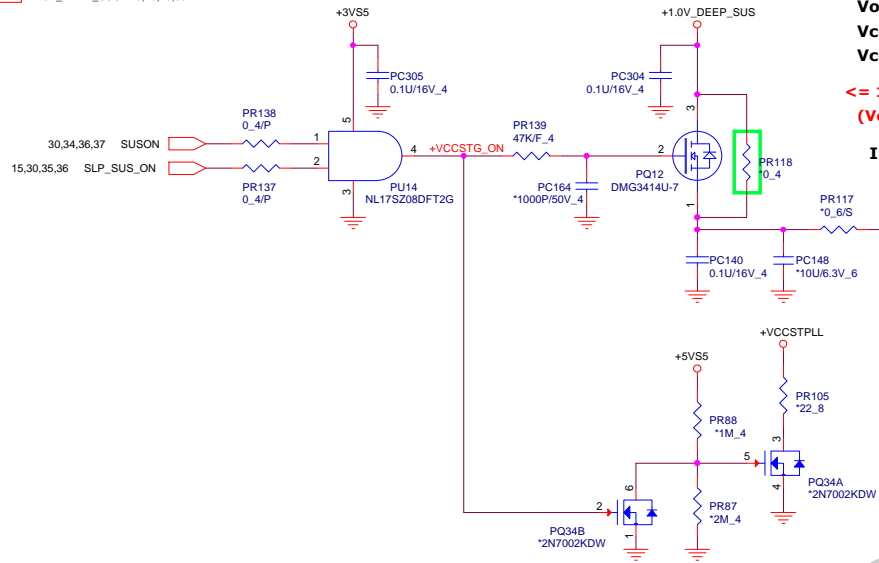
+VIN 20,27,32,33,34,38,39,40  
 +3VS5 4,15,22,28,30,31,33,36,37  
 +5VS5 4,25,33,34,36,37,38,39,40  
 +1.0V\_DEEP\_SUS 9,13,15,36  
 +1.8V\_DEEP\_SUS 9,15,37




**PROJECT : Y0DD**  
**Quanta Computer Inc.**

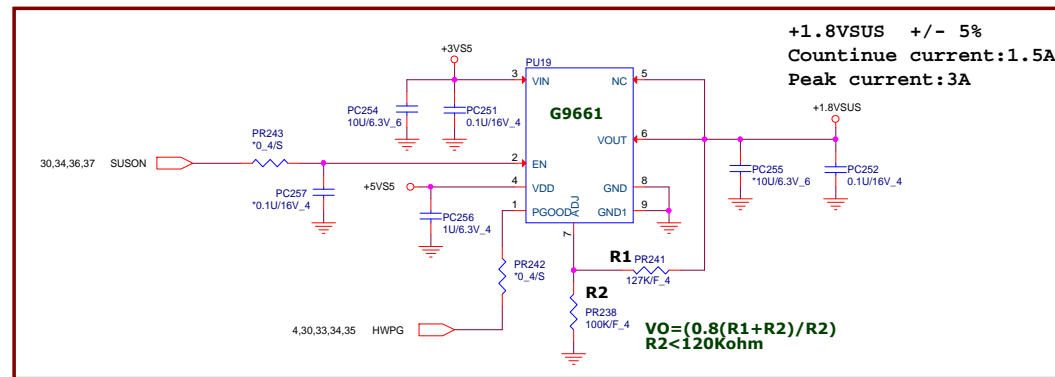
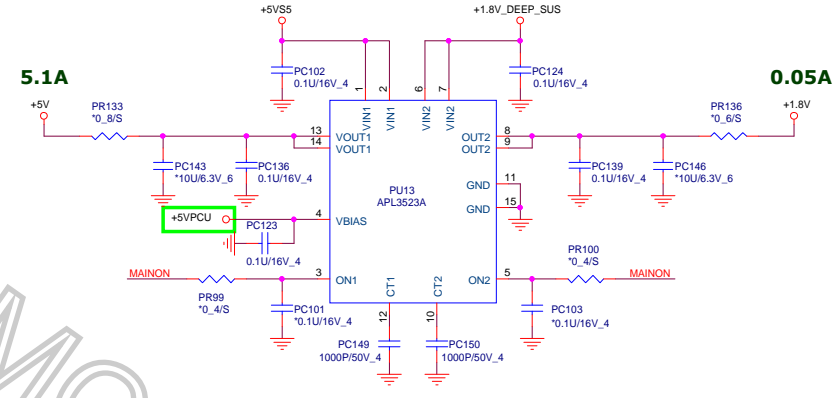
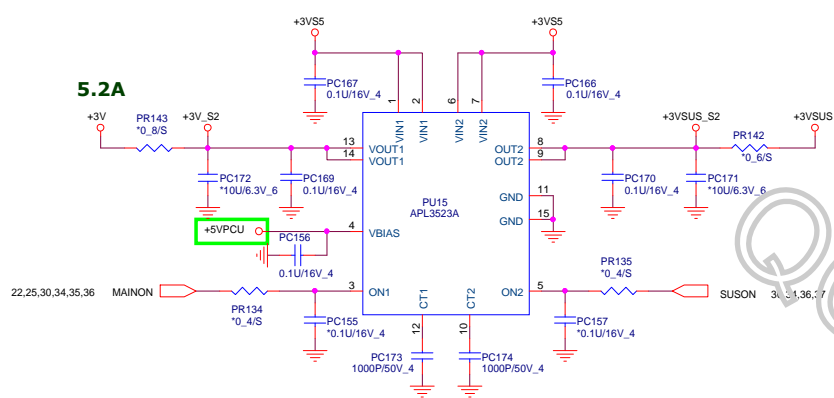
Size Custom	Document Number <b>+1.0/+1.5V/+1.8V_DEEP_SUS</b>	Rev 1A
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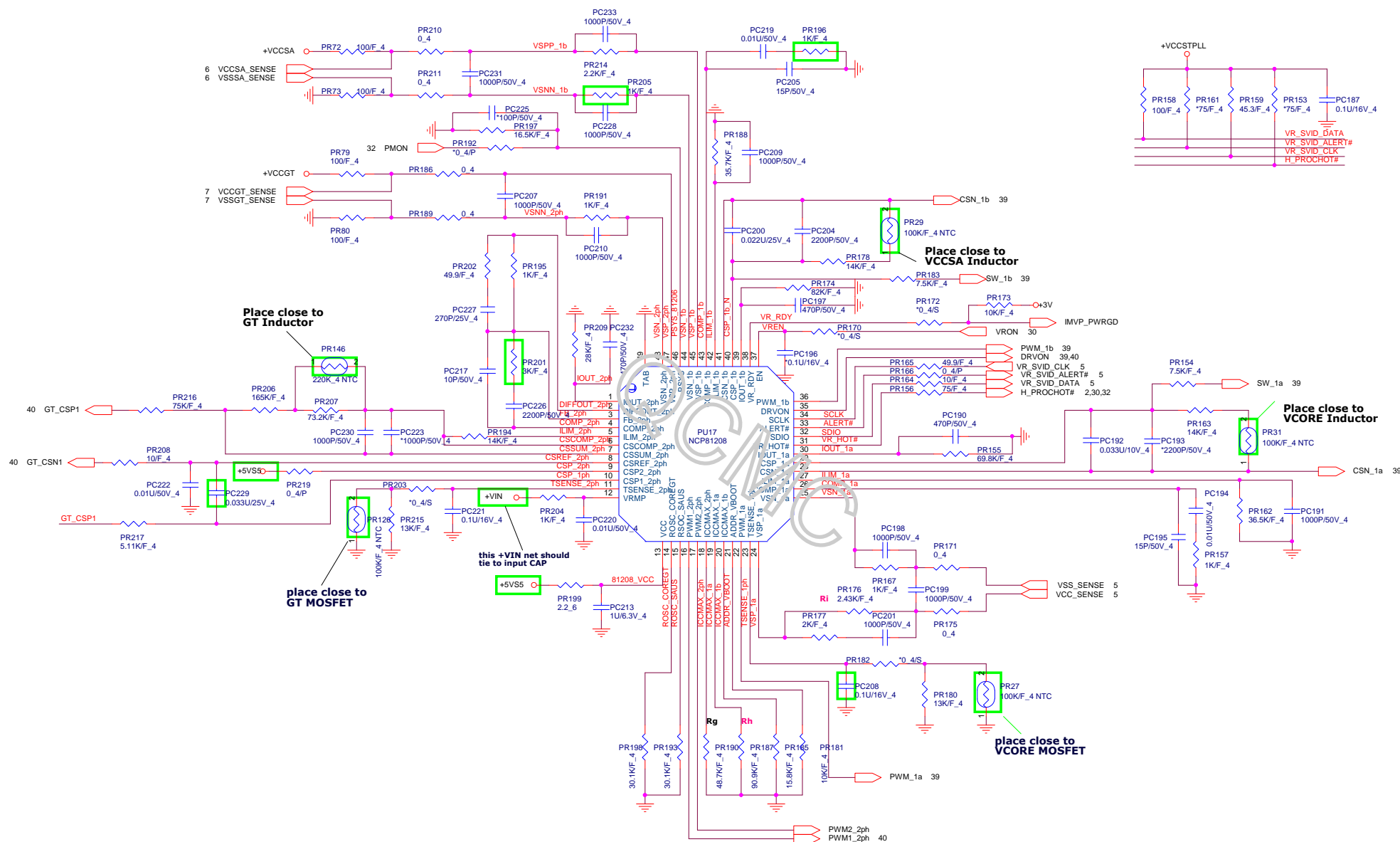
+1.0V 2,4,6,30  
 +3VS5 4,15,22,28,30,31,33,35,37  
 +5VS5 4,25,33,34,35,37,38,39,40  
 +VCCIO 2,6,16  
 +VCCSTPLL 2,5,6,9,38  
 +1.0V\_DEEP\_SUS 9,13,15,35

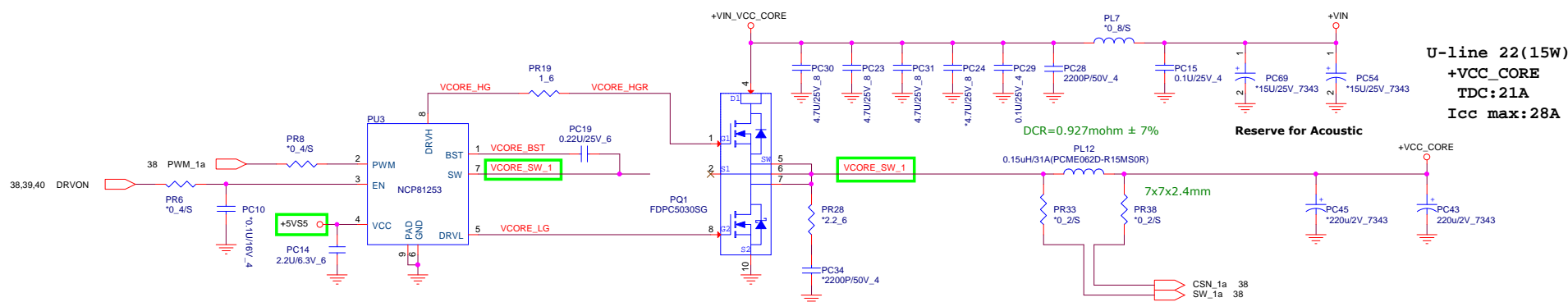


	<b>PROJECT : YODD</b>		
	Quanta Computer Inc.		
	Size Custom	Document Number <b>+1.0V/+VCCSTPLL</b>	Rev 1A
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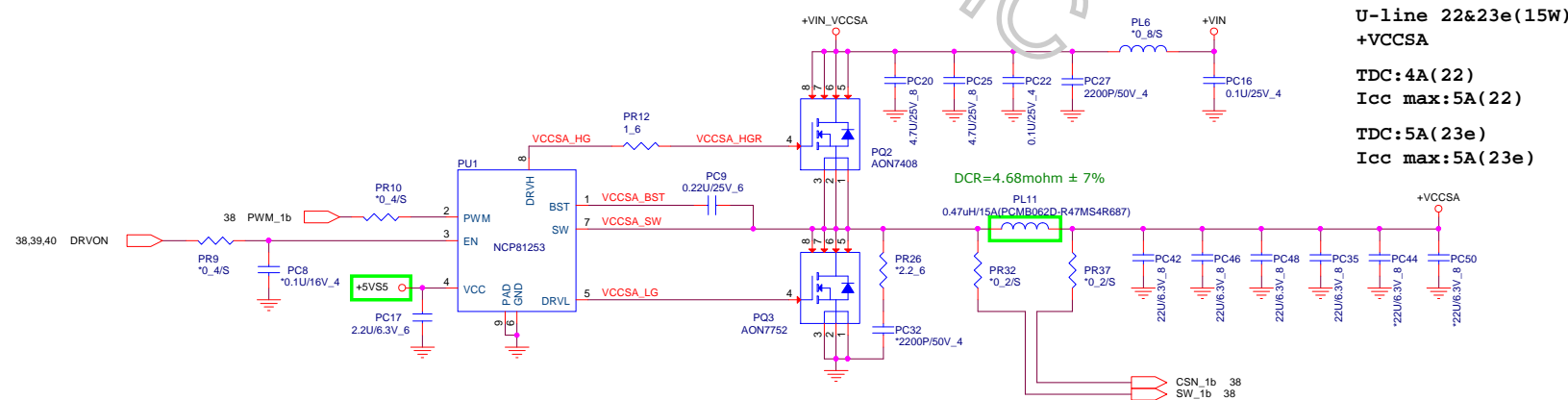
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+5V	22,23,24,27,37
+3VS5	4,15,22,28,30,31,33,35,36
+5VS5	4,25,33,34,35,36,38,39,40
+3VSUS	27,28
+1.8V_DEEP_SUS	9,15,35
+1.8V	23
+5V	22,23,24,27,37
+VIN	20,27,32,33,34,35,38,39,40
+1.8VSUS	17,18

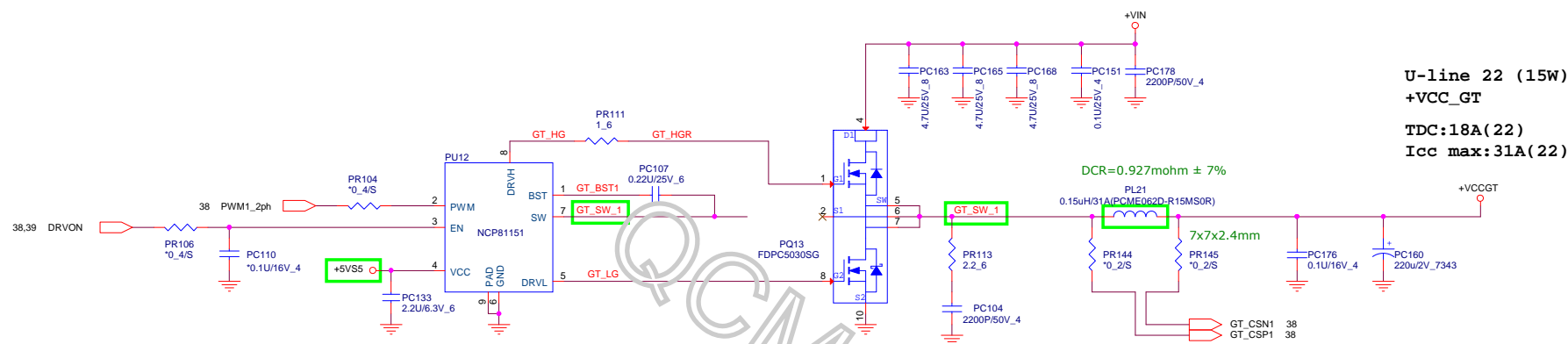






## VCCSA





```
U-line 22 (15W)
+VCC_GT

TDC:18A(22)
Icc max:31A(22)
```